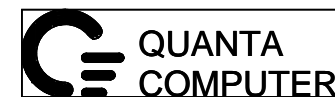


PCIE_REQ1#	PCIE_L0	PCIE_L6
PCIE_REQ2#	PCIE_L1	PCIE_L8
PCIE_REQ3#	PCIE_L2	PCIE_L4
PCIE_REQ4#	PCIE_L3	PCIE_L5 PCIE_L7

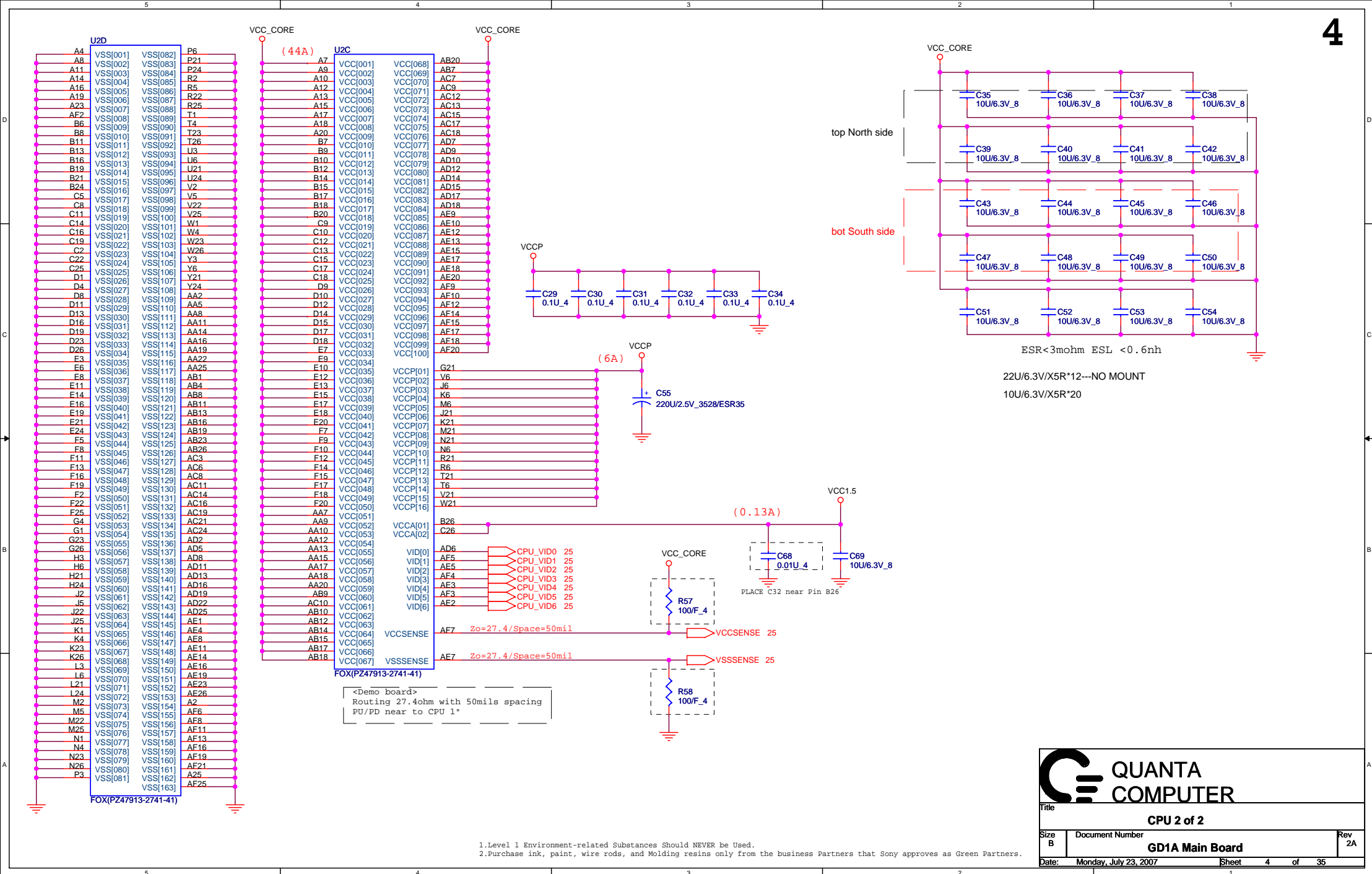


Title			
CLOCK GENERATOR			
Size B	Document Number		Rev 2A
	GD1A Main Board		
Date:	Monday, July 23, 2007	Sheet	2 of 35


FSC BSEL2	FSB BSEL1	FSA BSEL0	CPU	SRC	PCI	REF	USB	DOT	Spread %
0	0	0	266.66	100	33.33	14.318	48	96	0.5 Down
0	0	1	133.33	100	33.33	14.318	48	96	0.5 Down
* 0	1	0	<b>200.00</b>	100	33.33	14.318	48	96	0.5 Down
0	1	1	166.66	100	33.33	14.318	48	96	0.5 Down
1	0	0	333.33	100	33.33	14.318	48	96	0.5 Down
1	0	1	100.00	100	33.33	14.318	48	96	0.5 Down
1	1	0	400.00	100	33.33	14.318	48	96	0.5 Down
1	1	1	200.00	100	33.33	14.318	48	96	0.5 Down

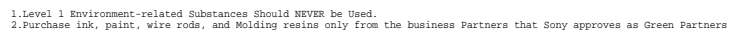
1. Level 1 Environment-related Substances should NEVER be Used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



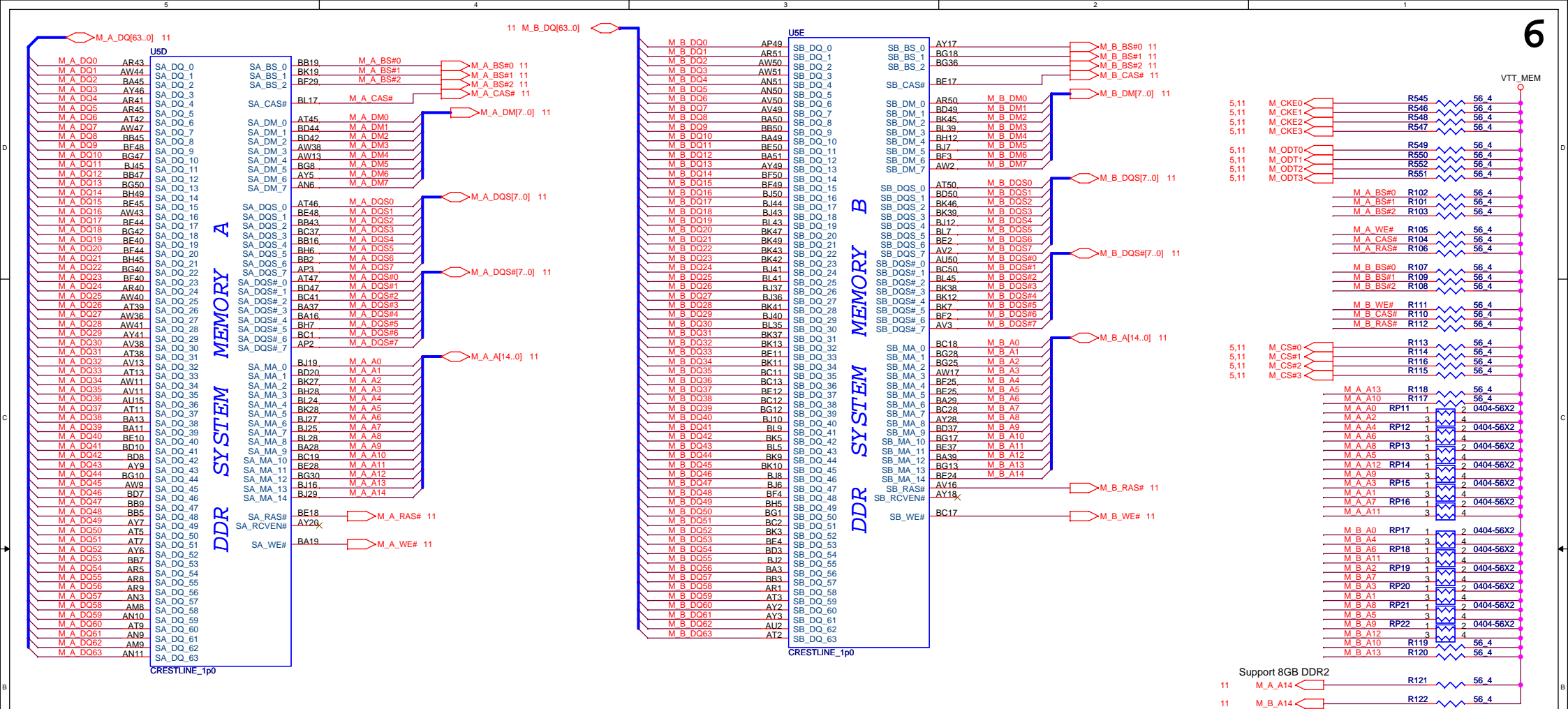


- 1.Level 1 Environment-related Substances Should NEVER be Used.
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 <b>QUANTA COMPUTER</b>	
Title	
CPU 2 of 2	
Size B	Document Number
GD1A Main Board	
Date:	Monday, July 23, 2007
Sheet	4 of 35
Rev 2A	

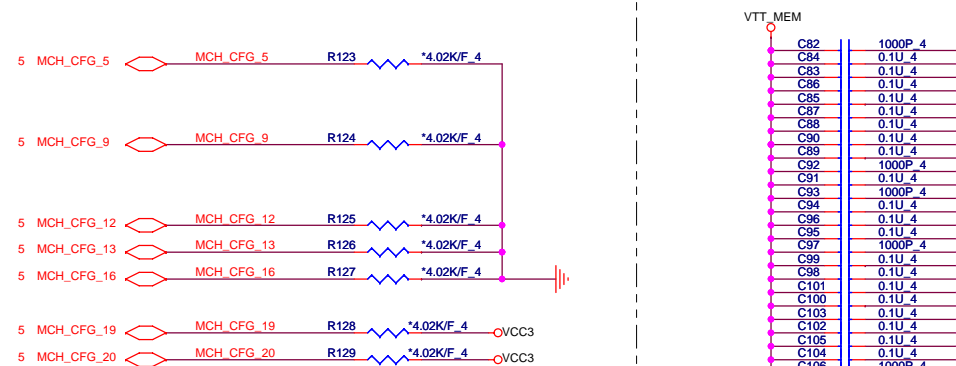






### GMCH Strap pin description

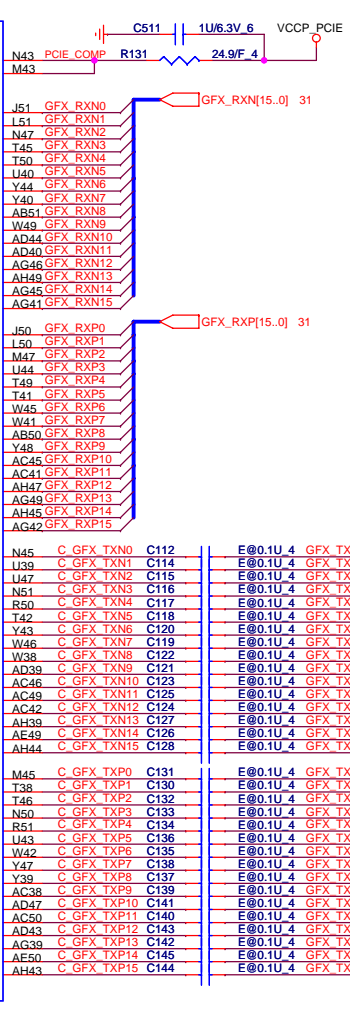
Low		High
CGF5	DMix2	* DMix4
CGF6	RSVD for 945GMS	
CGF7	RSVD	* CPU type: Mobile CPU
CGF9	PCIe Graphics lan : Reverse Lane	* PCIe Graphics lan : Normal operation
CGF10	reserved	
CGF11	reserved	
CGF16	FSB Dynamic ODT Disabled	* FSB Dynamic ODT Enabled
CGF18	* GMCH core: 1.05V	GMCH core: 1.5V
CGF19	* DMI LANE Normal	DMI LANE Reversed
CGF20	* only SDVO or PCIe x1 is operational	SDVO and PCIe x1 are operation simultaneously via the PEG port
CGF[13:12]		
00 = Partial clock gating disable 01 = XOR mode enabled 10 = All-Z mode enabled * 11 = <b>Normal Operation(Default)</b>		
Int.Pull-down : CFG 18,19,20 Int.Pull-high : CFG CFG 3-17		



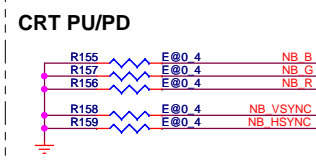
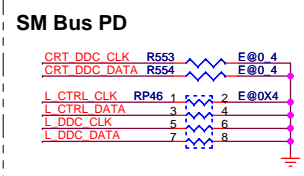
- Place one cap close to every 2 pull-up resistors terminated to VccSus0\_9 (Total 0.1 $\mu$  x 26)



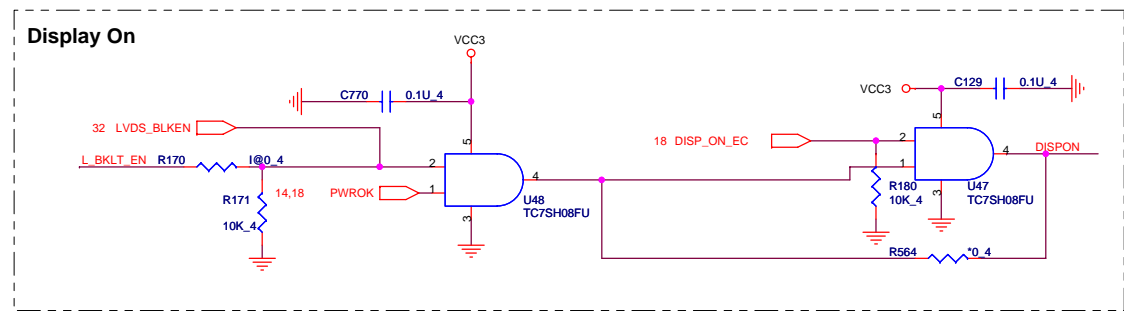
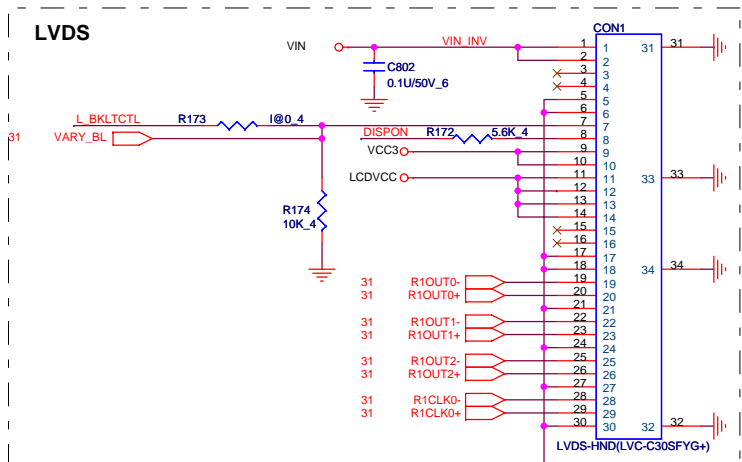
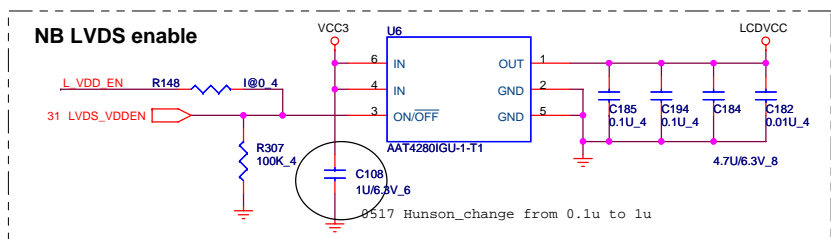
Title			
GMCH DDR II 2 of 5			
Size	Document Number		Rev
	GD1A Main Board		2A
Date:	Monday, July 23, 2007	Sheet	6 of 35



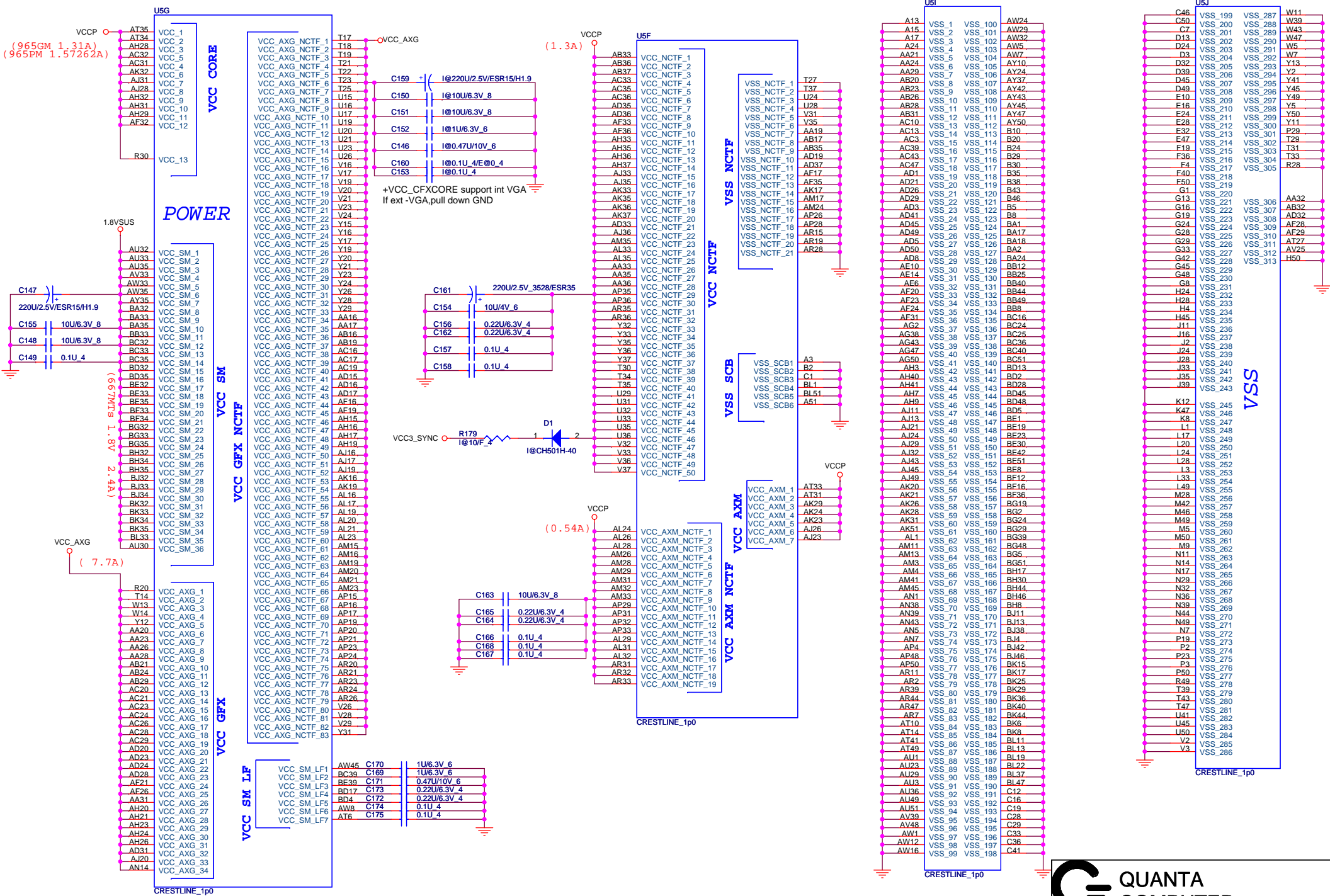
Signal		GM965	PM965
NB_VSYNC	R158	NI	0_4
	R168	30_1_4	NI
NB_HSYNC	R159	NI	0_4
	R166	30_1_4	NI
GFX	C112, C114~C129, C130~C145	NI	0.1UF_4



Signal		965GM	965PM
NB_B	R160	0_4	NI
	R155	150_4	0_4
NB_G	R161	0_4	NI
	R157	150_4	0_4
NB_R	R162	0_4	NI
	R156	150_4	0_4
L_IBG	R147	2.4K_4	NI
LVDS	RP38	0X2	NI
	RP41~RP43		
L_BKLT_EN	R170	0_4	NI
L_CTRL_CLK	R130	10K	NI
	RP46	NI	0X4
L_CTRL_DATA	R145	10K	NI
	RP46	NI	0X4
LVDS_VDDEN	R146	0_4	NI
DDC2BC	R163	0_4	NI
	R553	NI	0_4
DDC2BD	R164	0_4	NI
	R554	NI	0_4
CRT_TVO_IREF	R167	1.3K_4	0
L_DDC_CLK	RP46	NI	0X4
L_DDC_DATA	RP46	NI	0X4
BRIGHT	R173	0_4	NI
	R175	NI	0_4

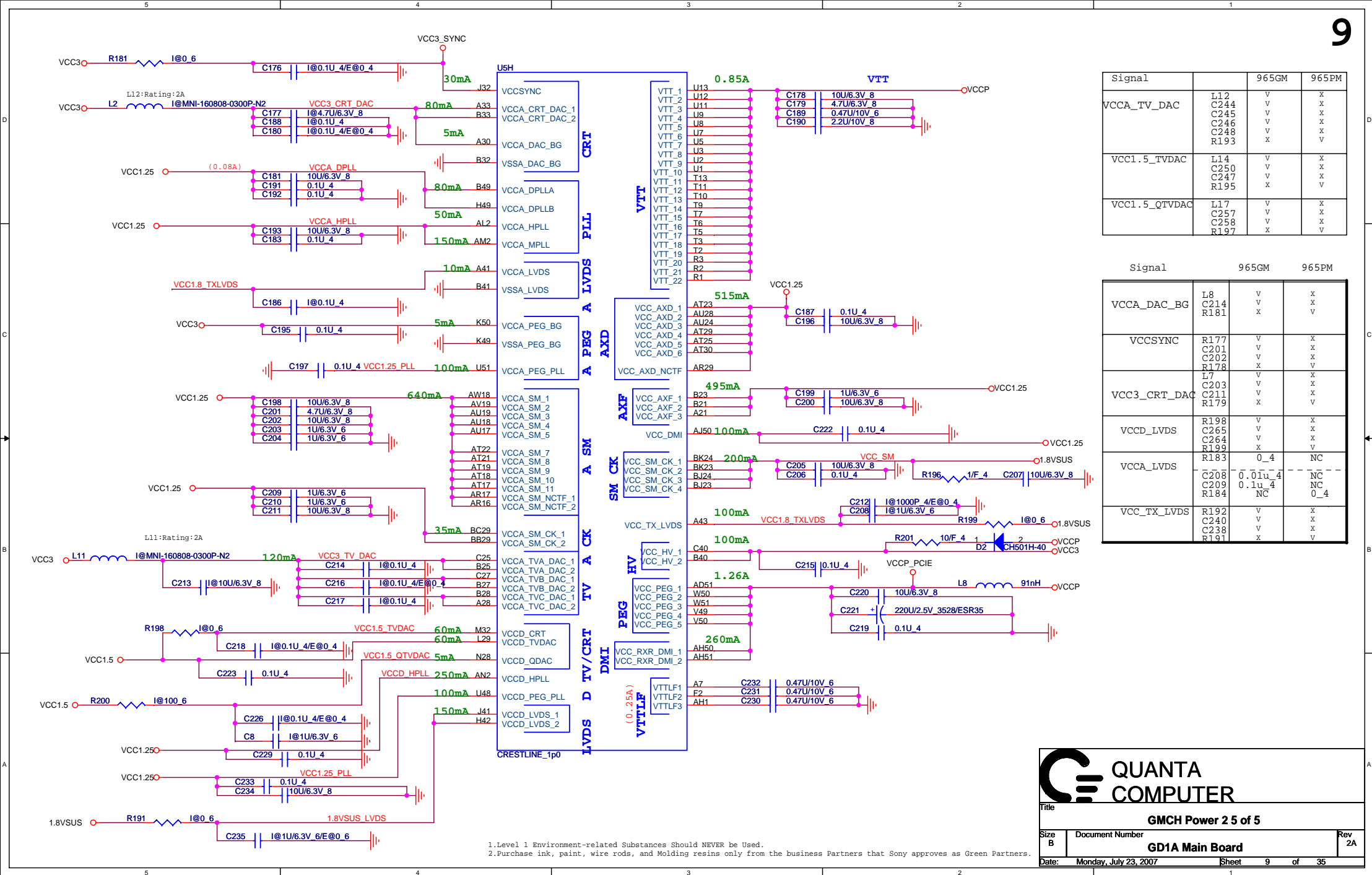


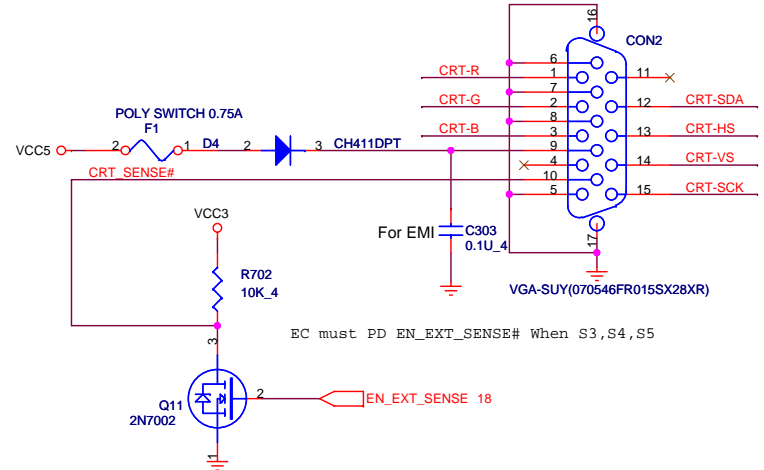
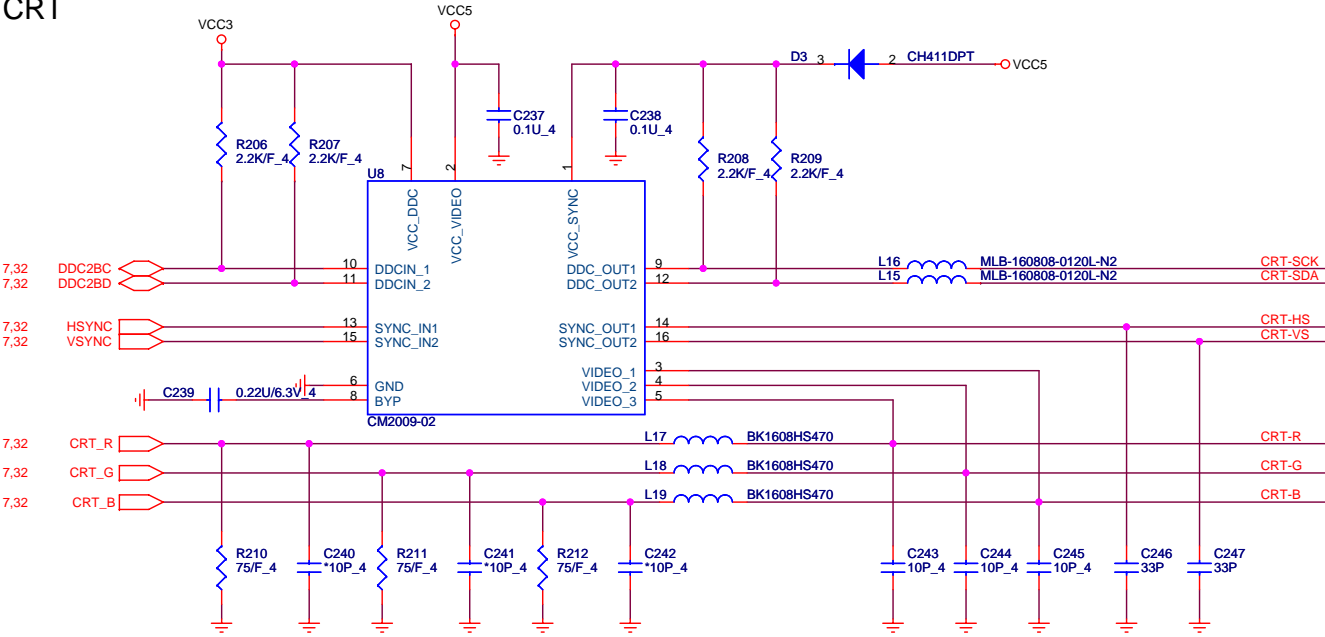
1.Level 1 Environment-related Substances Should NEVER be Used.  
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



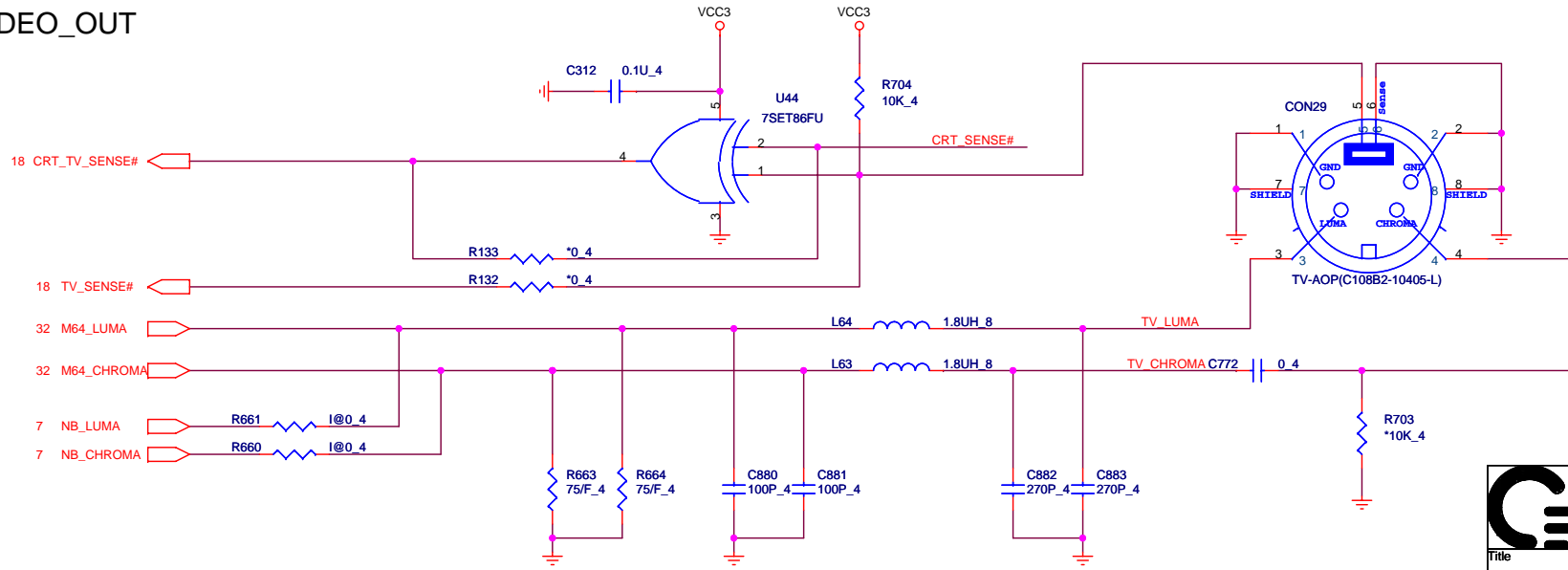
1. Level 1 Environment-related Substances Should NEVER be Used.  
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.








S-VIDEO\_OUT

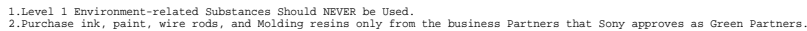


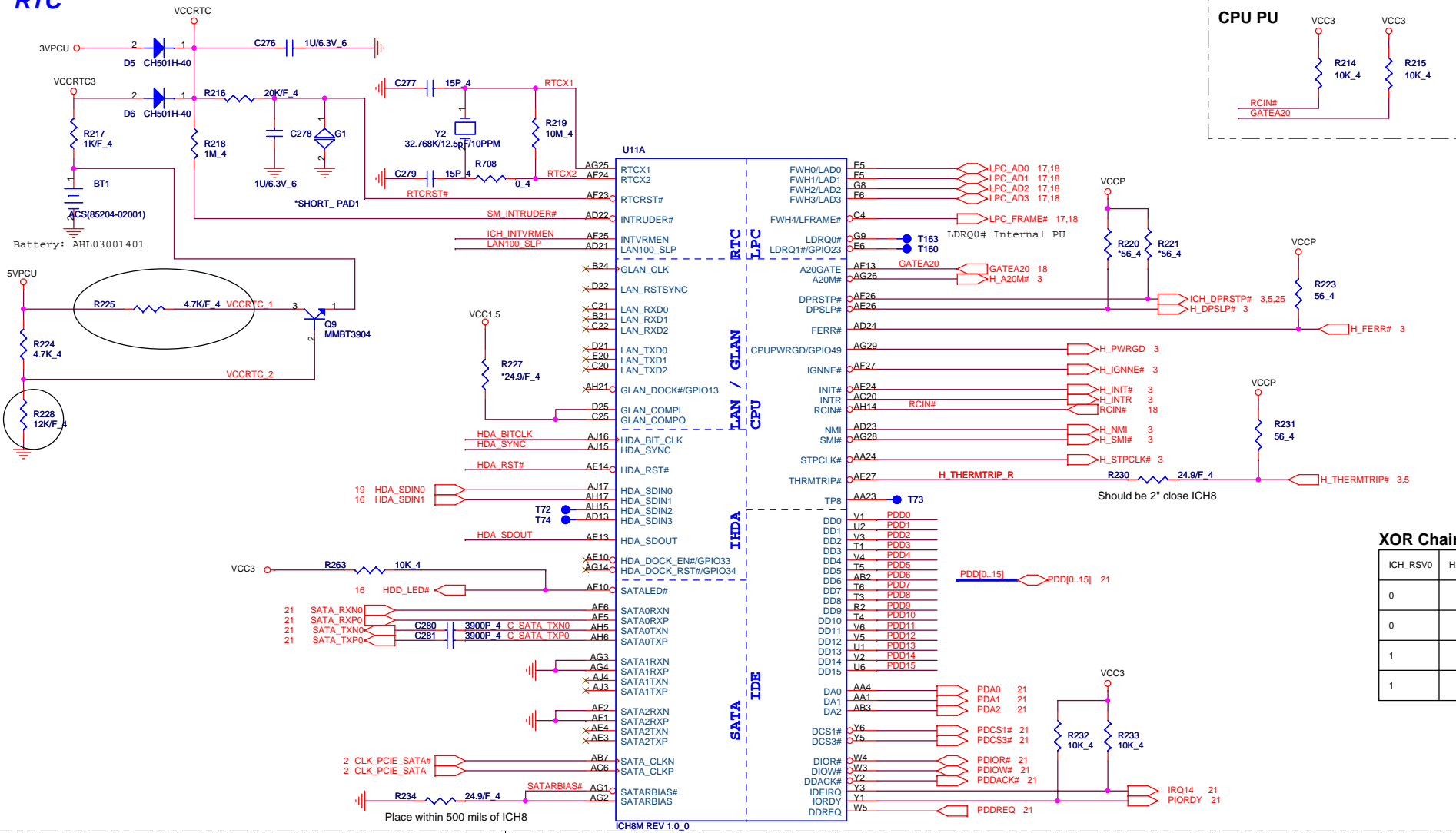


QUANTA  
COMPUTER

Title			CRT & S-VIDEO		
Size	Document Number				Rev
B			GD1A Main Board		2A
Date:	Monday, July 23, 2007	Sheet	10	of	35

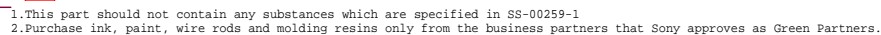
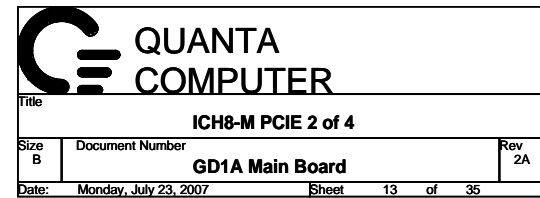
1.Level 1 Environment-related Substances Should NEVER be Used.  
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



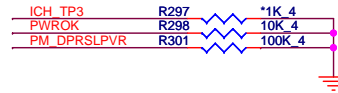
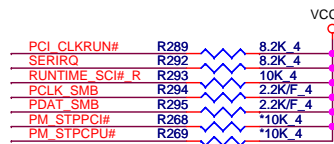
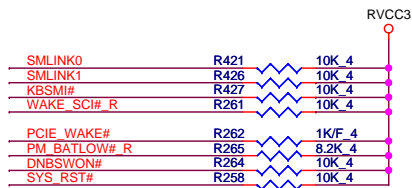


PCI_GNT#3	Low = A16 swap override enabled High = Default
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PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

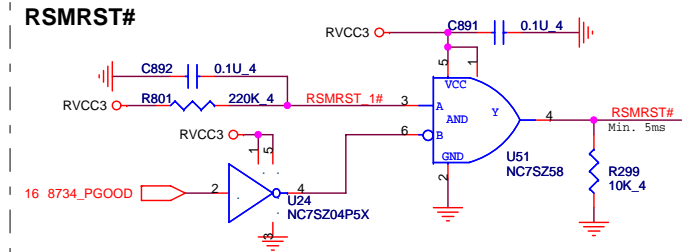






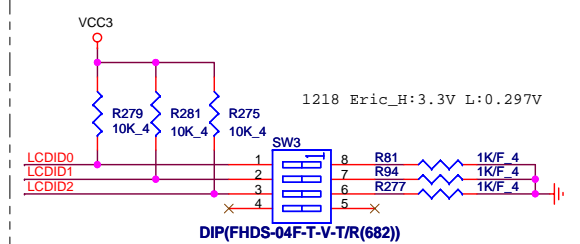
RSMRST# must be after RVCC3 10 ms

### RSMRST#

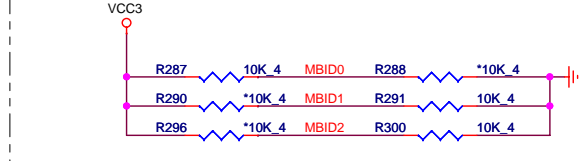


LCDID	Panel Type
X001	AUO -QD14TL0206
X010	CPT -CLAA141WB02A
X011	CPT -CLAA141WB05A

### LCD ID

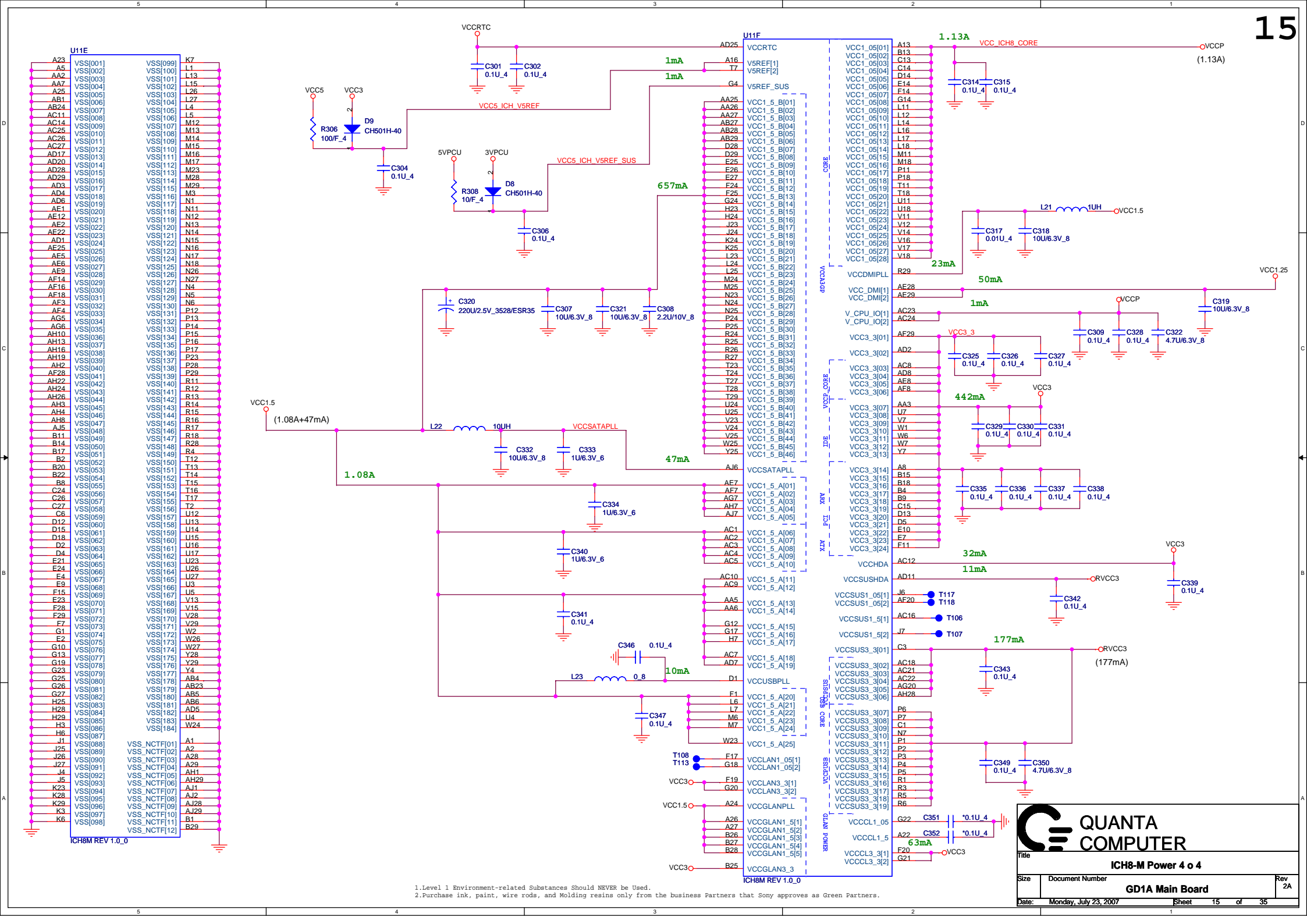


### MB ID

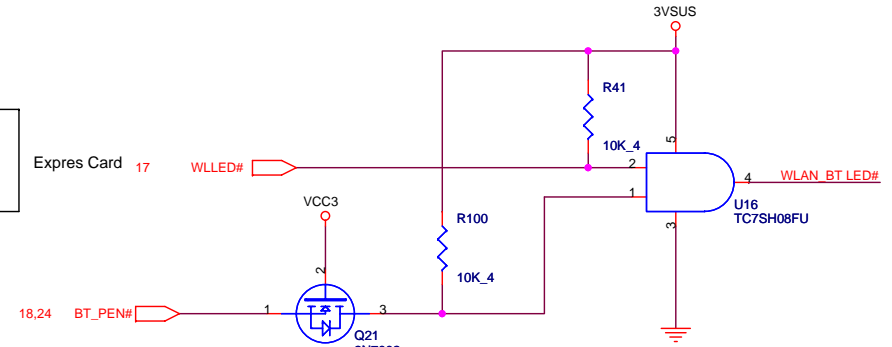
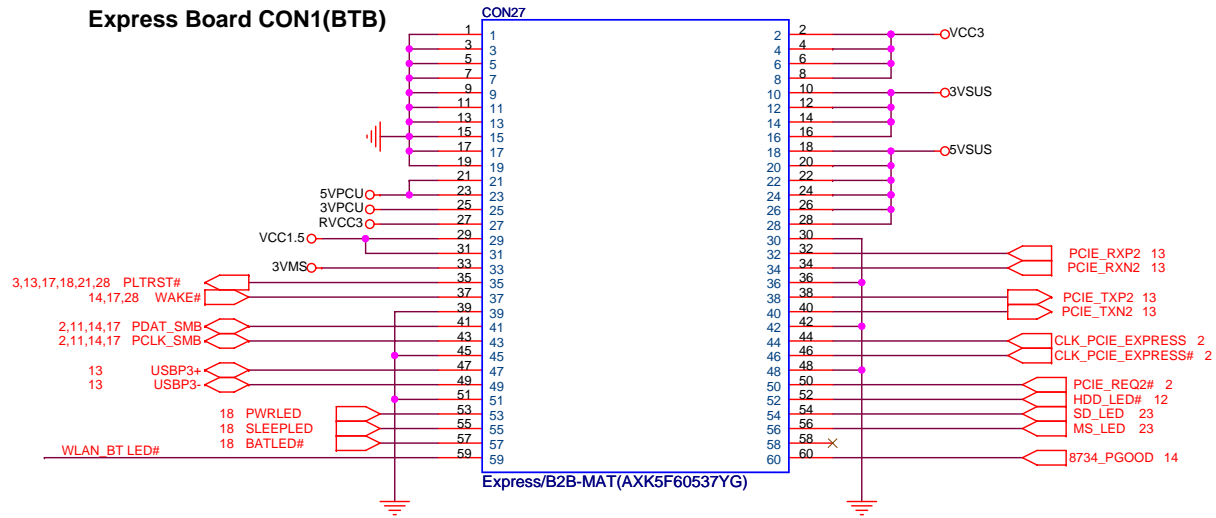


Title		
ICH8-M GPIO 3 of 4		
Size	Document Number	Rev
B	GD1A Main Board	2A
Date:	Monday, July 23, 2007	Sheet 14 of 35

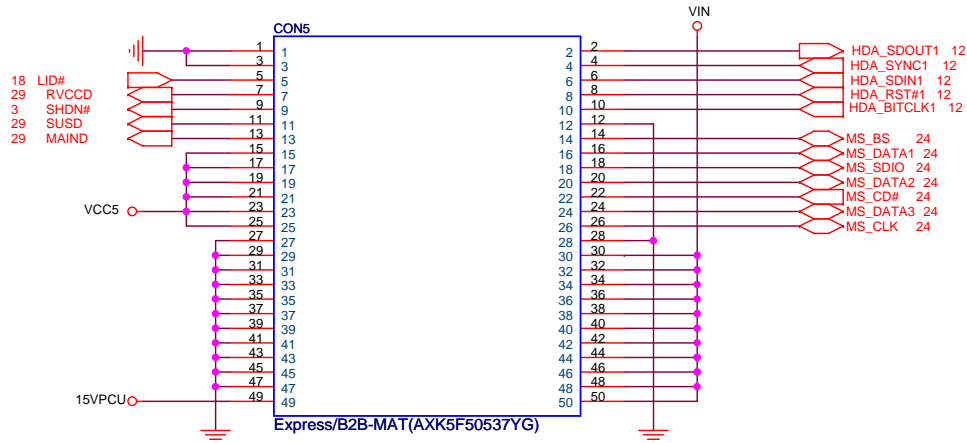
- Level 1 Environment-related Substances Should NEVER be Used.
- Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



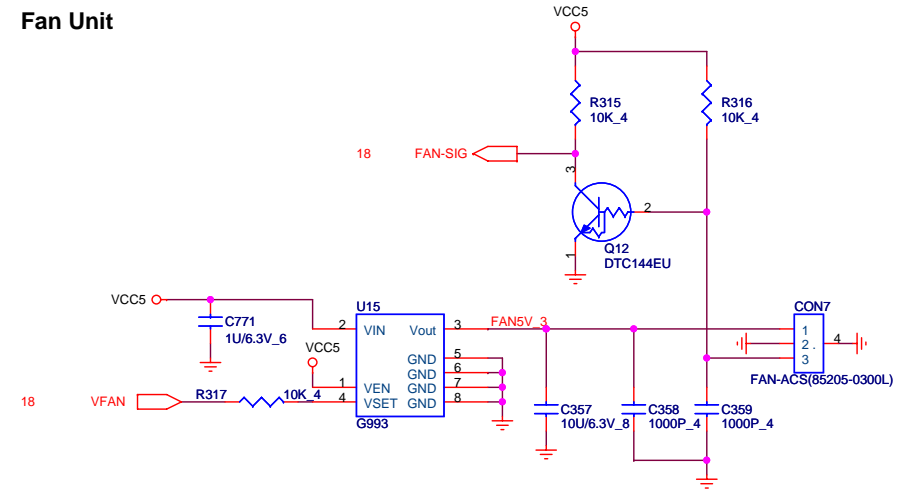
## Express Board CON1(BTB)



## Express Board CON2(BTB)



## Fan Unit



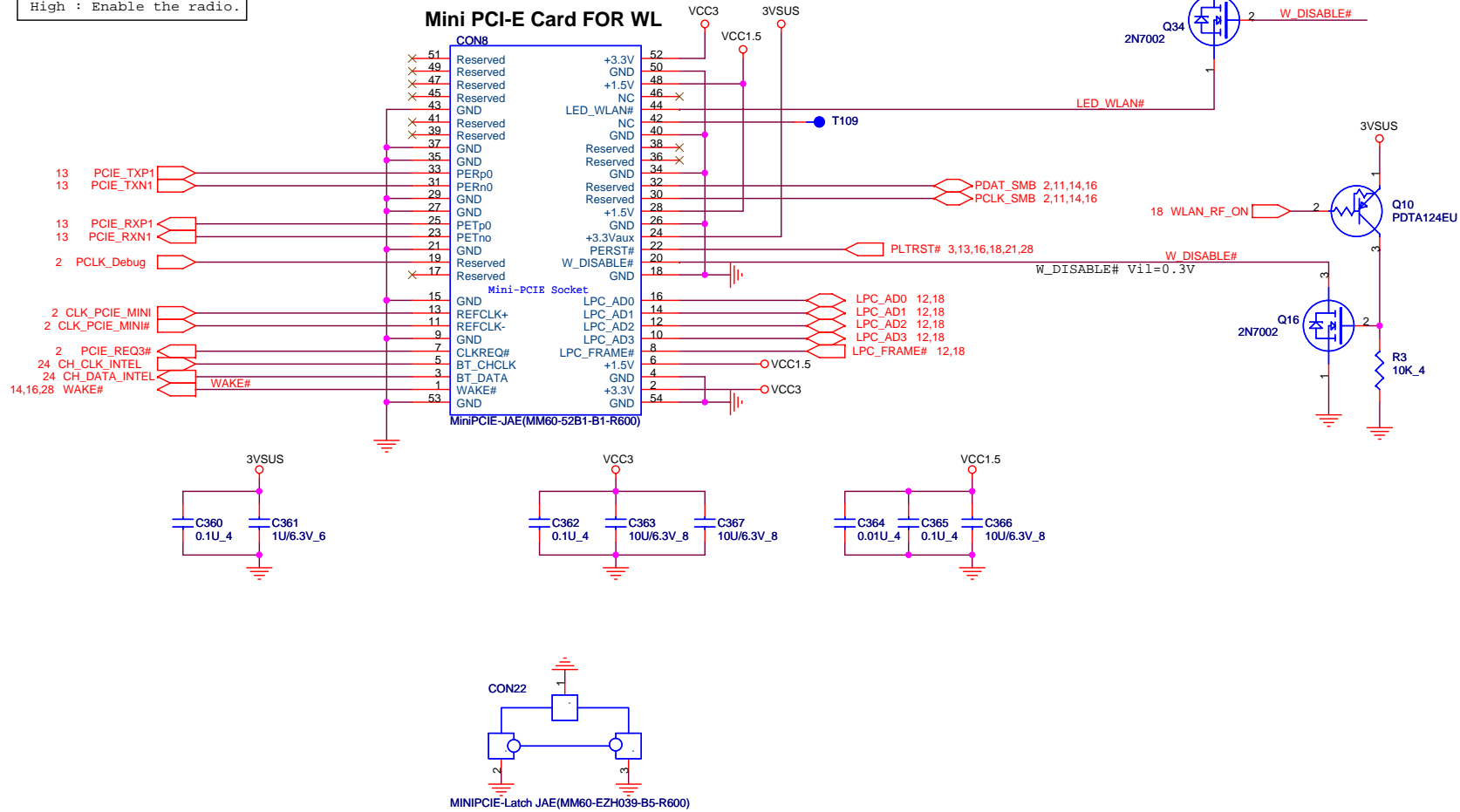
Title		
Express Card		
Size	Document Number	Rev
B	GD1A Main Board	2A
Date:	Monday, July 23, 2007	Sheet 16 of 35

- This part should not contain any substances which are specified in SS-00259-1
- Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.

LED\_GP :LED WLEN LINK  
Output Current : 7mA  
Blink rate : 1 flash per every 3 sec.

WLSW:  
Low : disable the radio.  
High : Enable the radio.

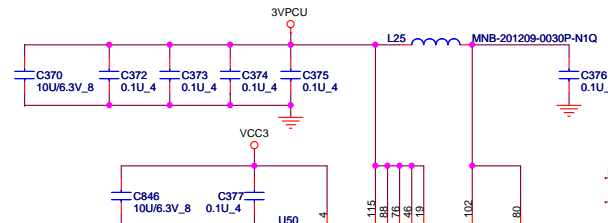
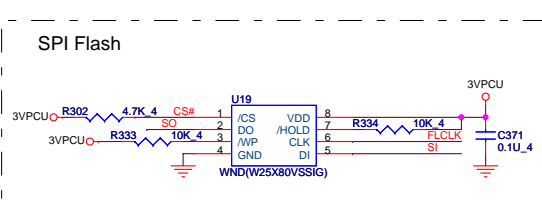
### Mini PCI-E Card FOR WL



1.Level 1 Environment-related Substances Should NEVER be Used.  
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

		QUANTA COMPUTER	
Title <b>MINIPCIE / MDC</b>			
Size B	Document Number <b>GD1A Main Board</b>		Rev 2A
Date:	Monday, July 23, 2007	Sheet	17 of 35

## SPI Flash



I/O Address	Index	Data
BADDR1-0	1 0	2E 2F
	1 1	4E 4F
0 0	HCFGBAH, HCFGBAL	(HCFGBAH, HCFGBAL)+1
0 1	XOR-TEST	

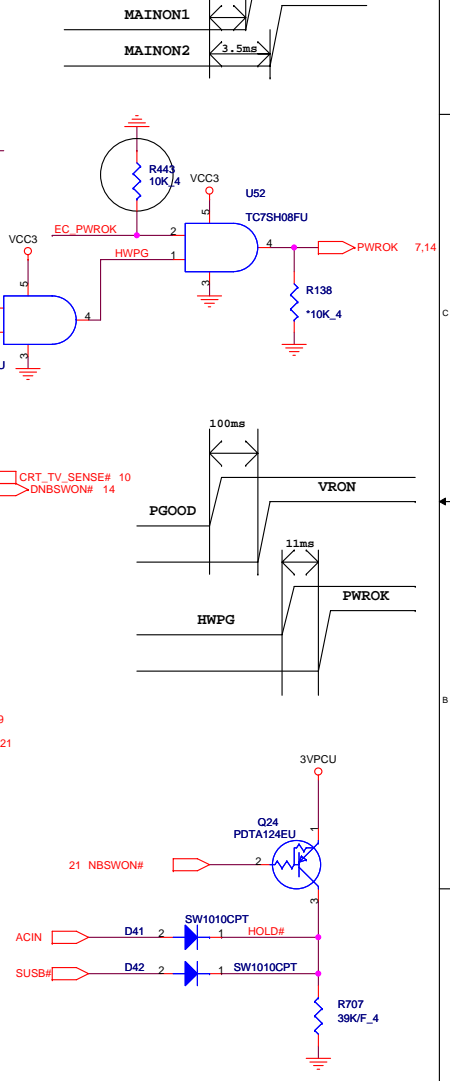
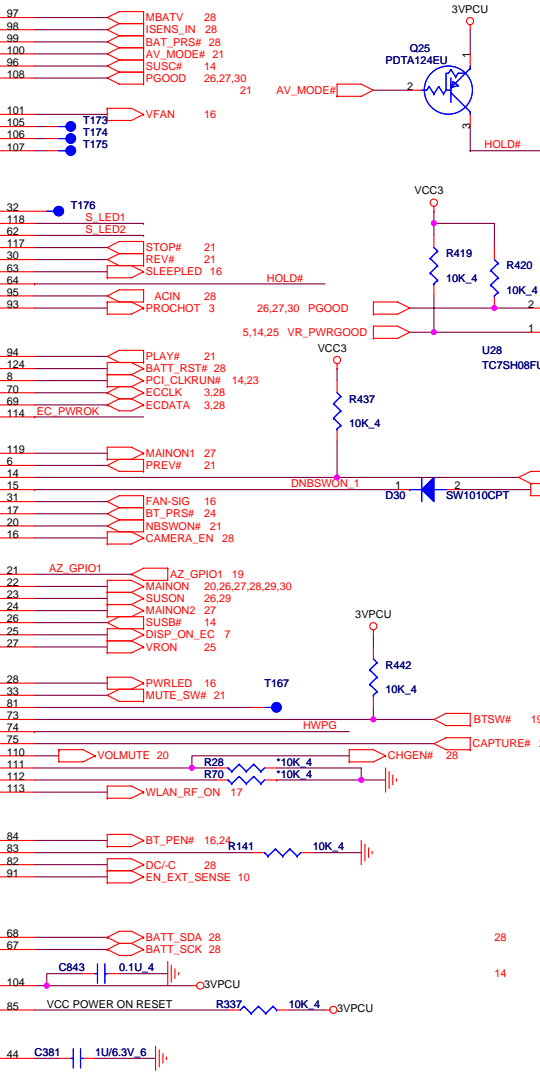
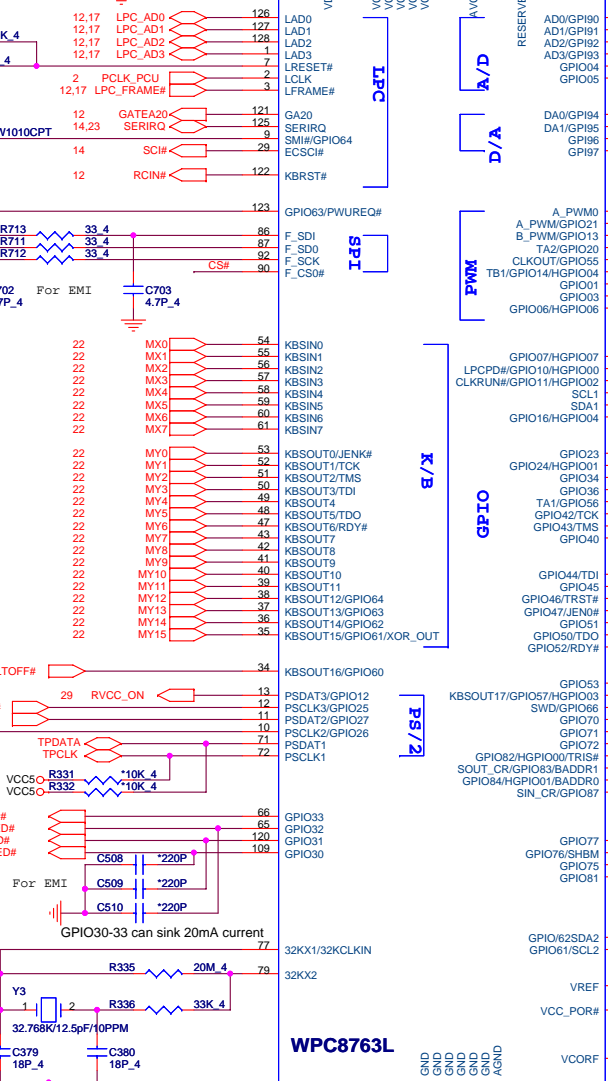
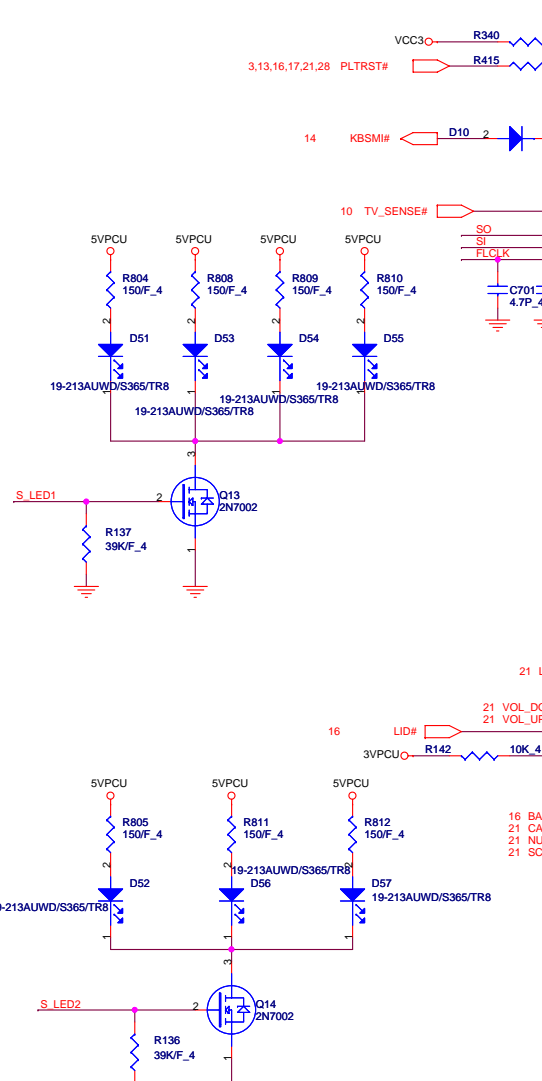
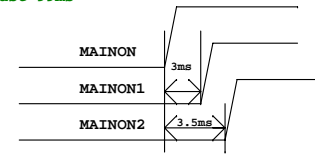
DOCK\_RST# \* BADDR0

DK\_RST\_PEN# BADDR1

BT\_PEN# : SHBM(If = 0 Enable share host BIOS memory)

PWROK must be after HWPG at least 10ms  
VRON must be after PGOD at least 99ms

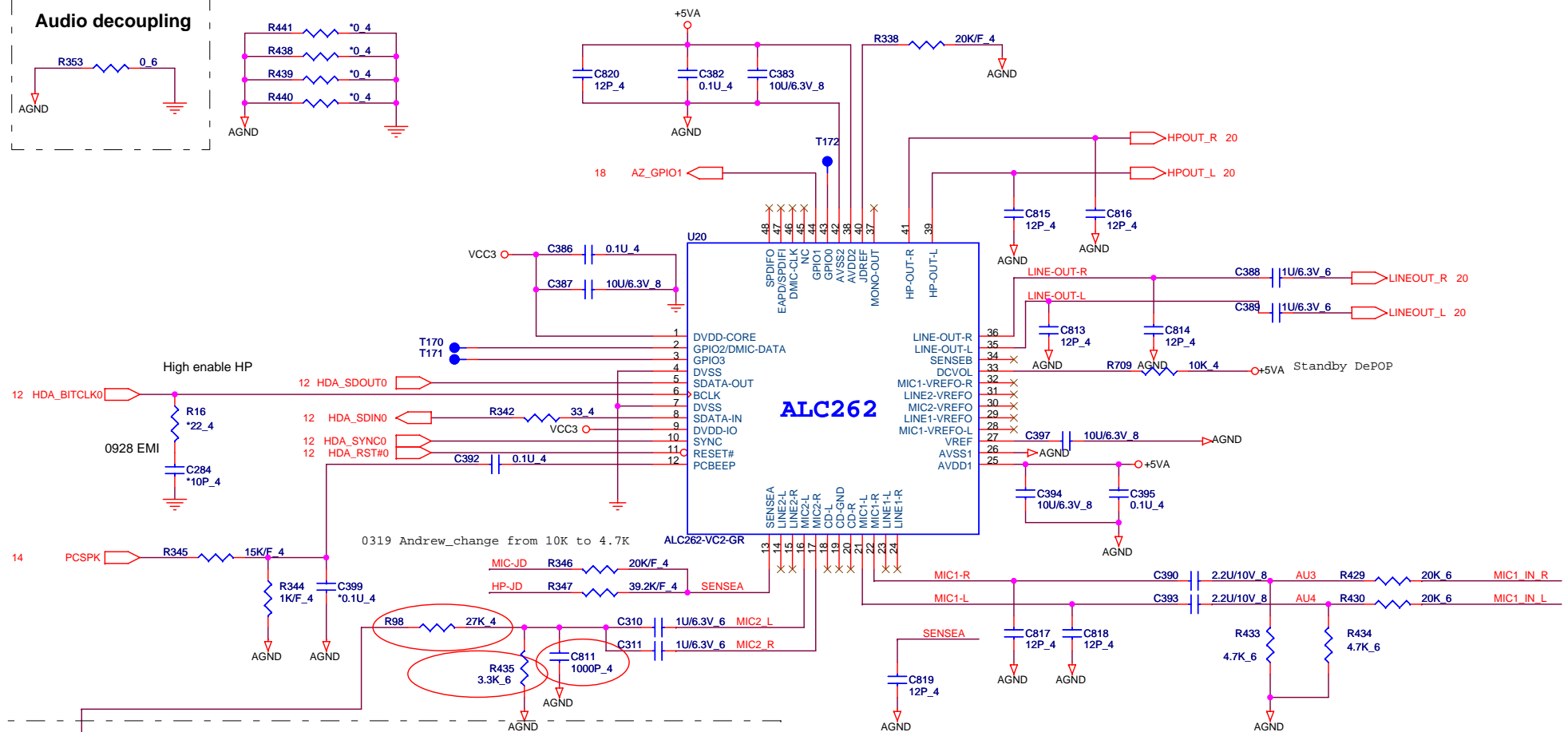
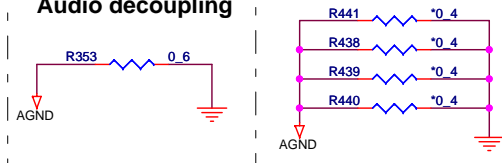
MAINON <-- 3ms --> MAION1  
MAINON <-- 3.5ms --> MAION2



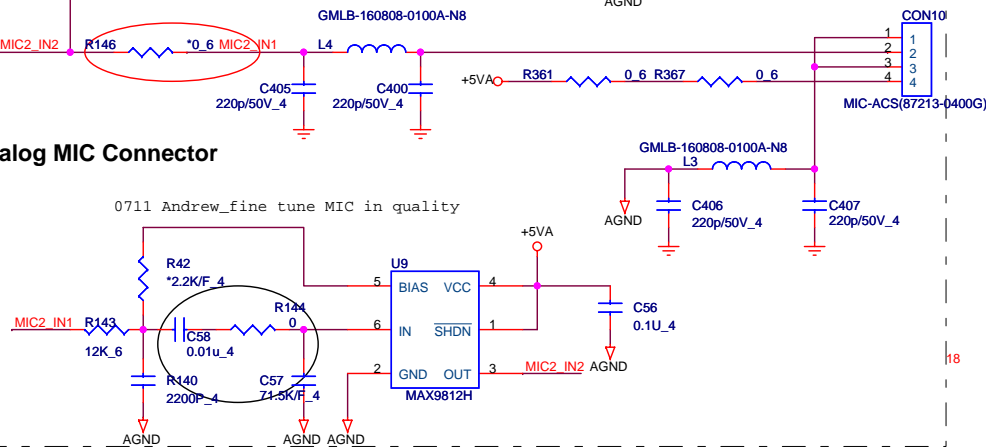
JEN0(PIN24)	JENK(PIN53)	Functionality of PINs (17,20,21,23,25,27)	Functionality of PINs (47,48,50,51,52)
NC	NC	GPIO	KEYBOARD OUTPUT
10K PD	NC	JTAG Signal	KEYBOARD OUTPUT
NC	10K PD	GPIO	JTAG Signal
10K PD	10K PD		Illegal Strap combination



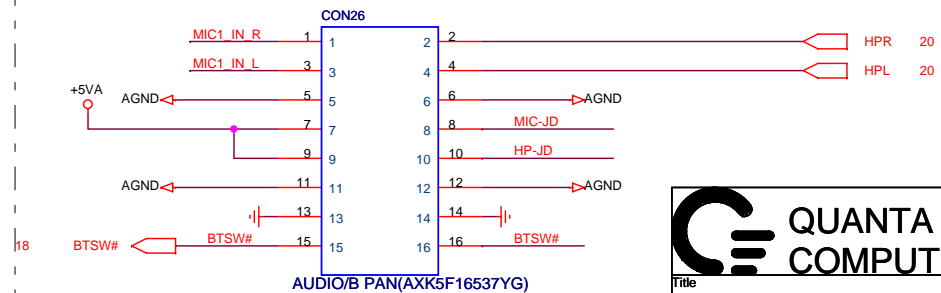
## Audio decoupling



## Analog MIC Connector

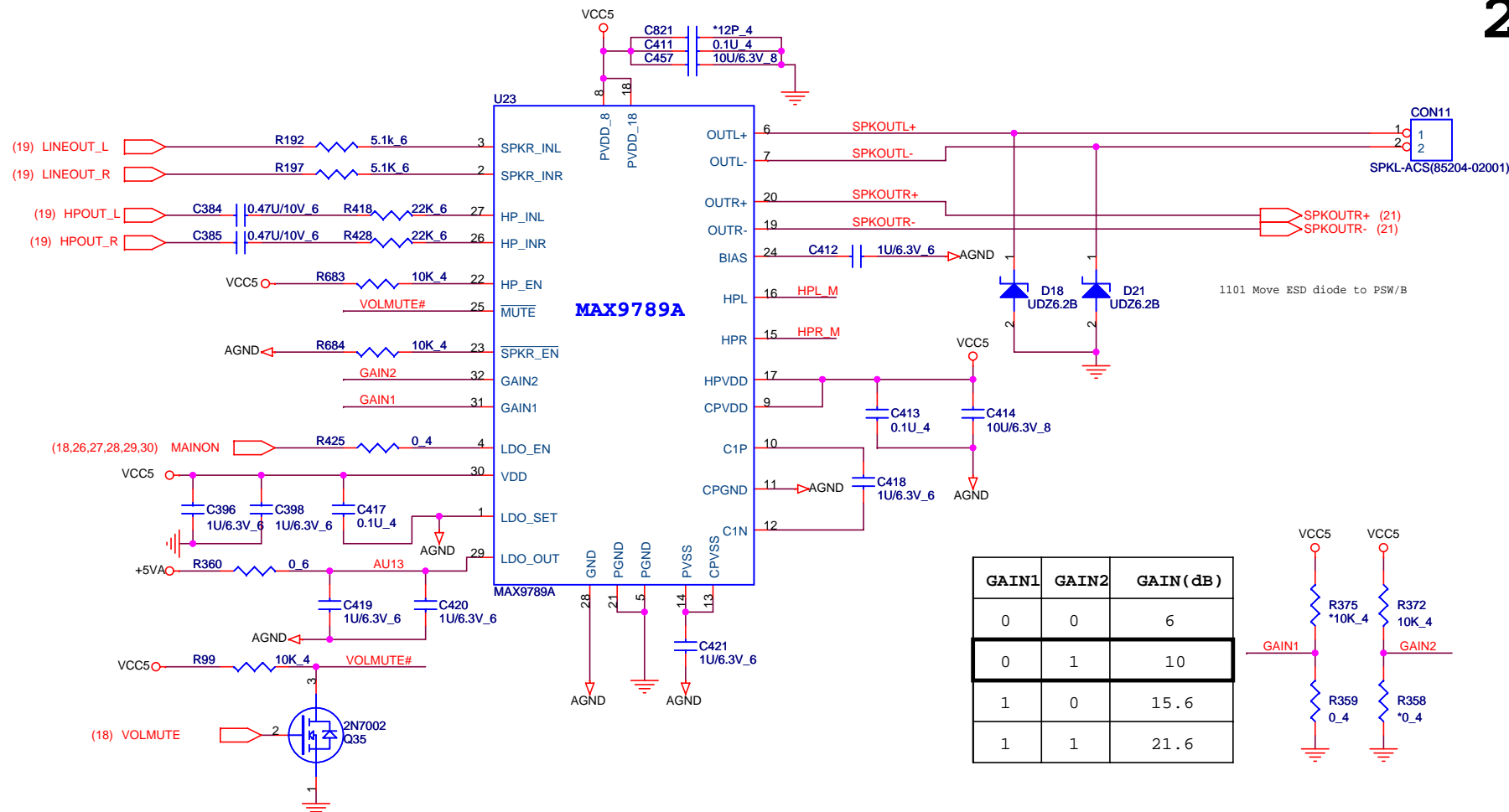


## Audio/B CON(B2B)

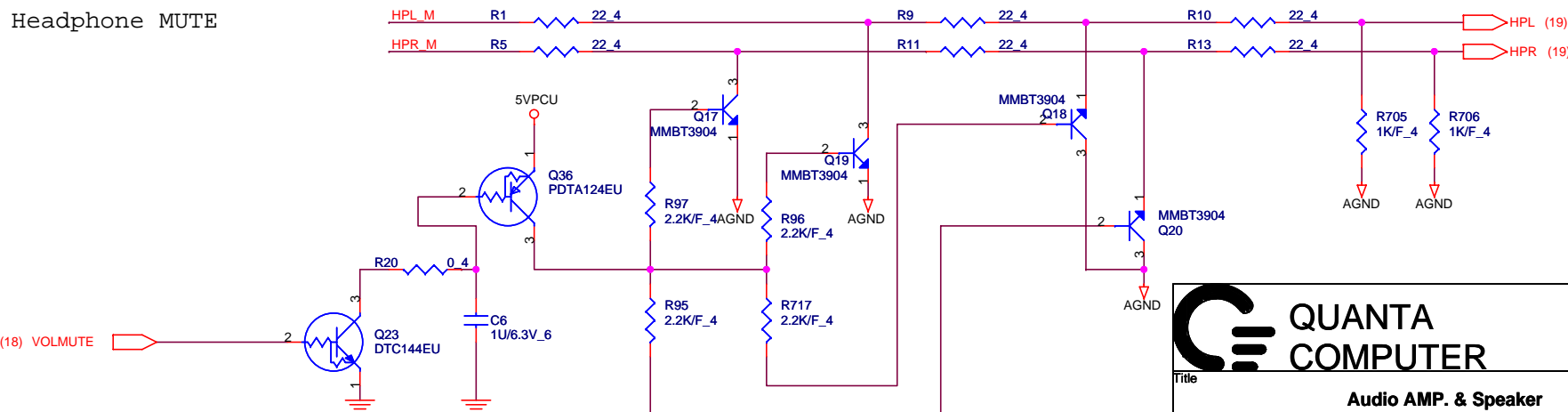


Title			Audio ALC268	
Size	Custom	Document Number	GD1A Main Board	
Date:	Monday, July 23, 2007	Sheet	19	of 35
			Rev	2A

1. Level 1 Environment-related Substances Should NEVER be Used.  
 2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



## Headphone MUTE



1.Level 1 Environment-related Substances Should NEVER be Used.  
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

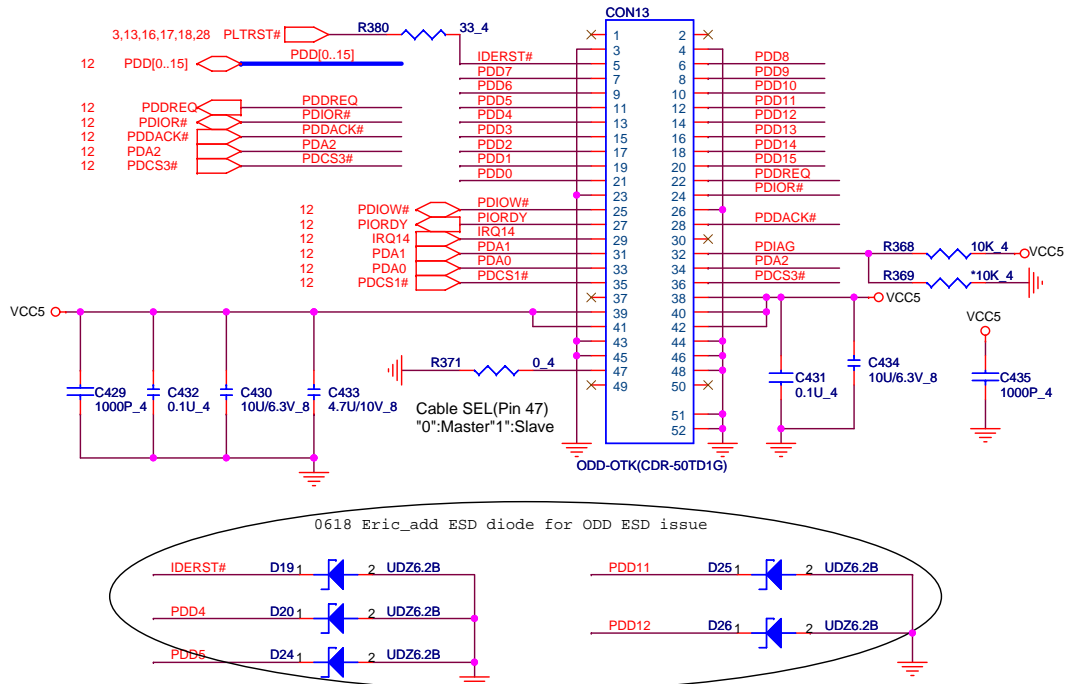
**QUANTA COMPUTER**

Title: **Audio AMP. & Speaker**

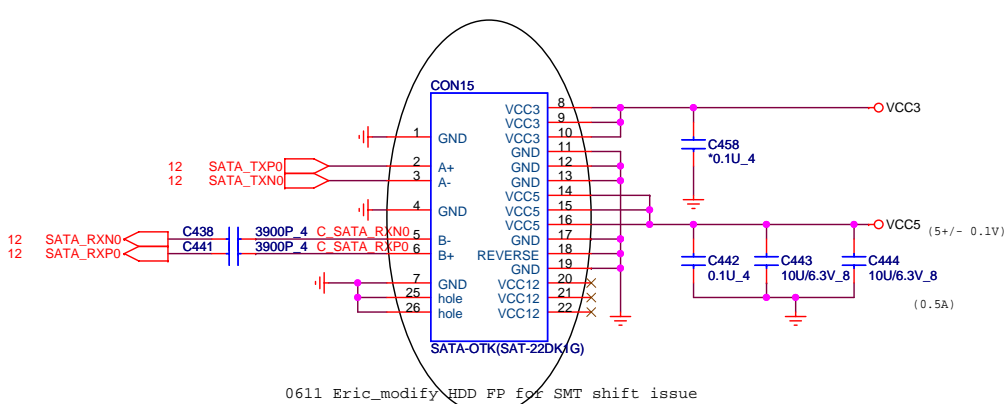
Size: Custom Document Number: **GD1A Main Board** Rev: 2A

Date: Monday, July 23, 2007 Sheet 20 of 35

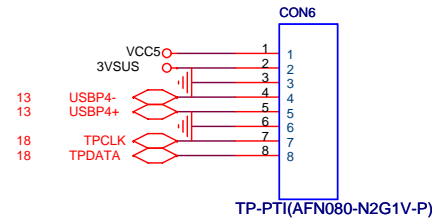
## ODD CONNECTOR



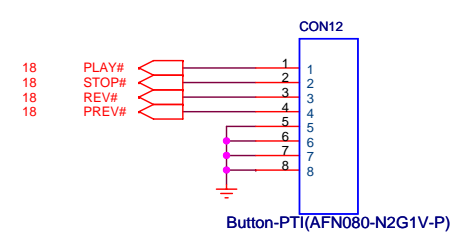
## HDD CONNECTOR



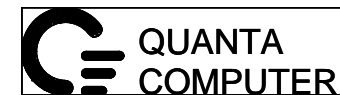
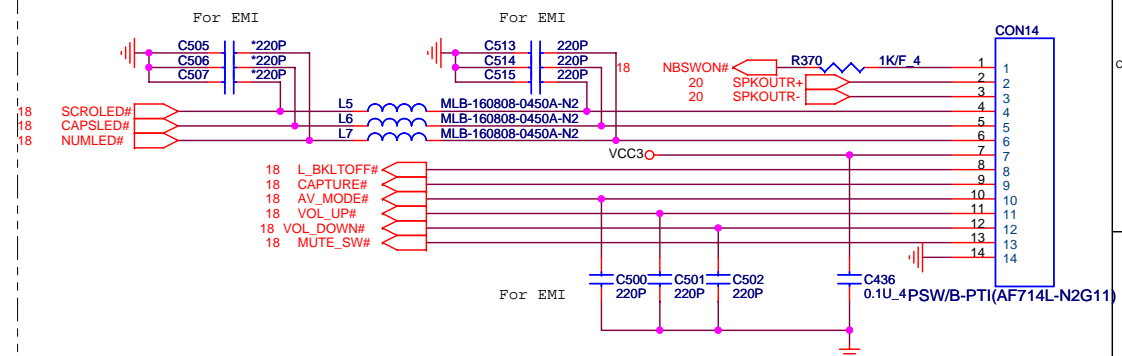
## TouchPAD Board CON(FPC)



## Button CON(FFC)

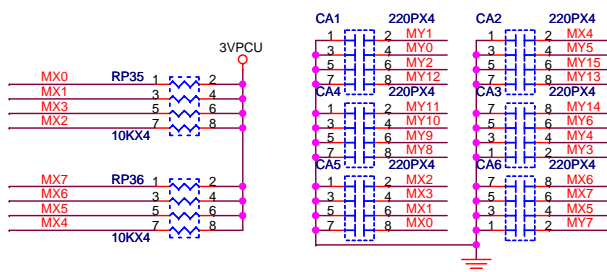
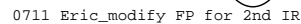


## PSW Board CON(Inverse FFC)



Title			HDD/ODD/PSW/BUT/TP
Size	Document Number		Rev
B	GD1A Main Board		3A
Date:	Monday, July 23, 2007	Sheet	21 of 35

- 1.Level 1 Environment-related Substances Should NEVER be Used.
- 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



13  
13

5VSUS

C466

1U/6.3V

6

CON20

6

5

4

4

3

2

2

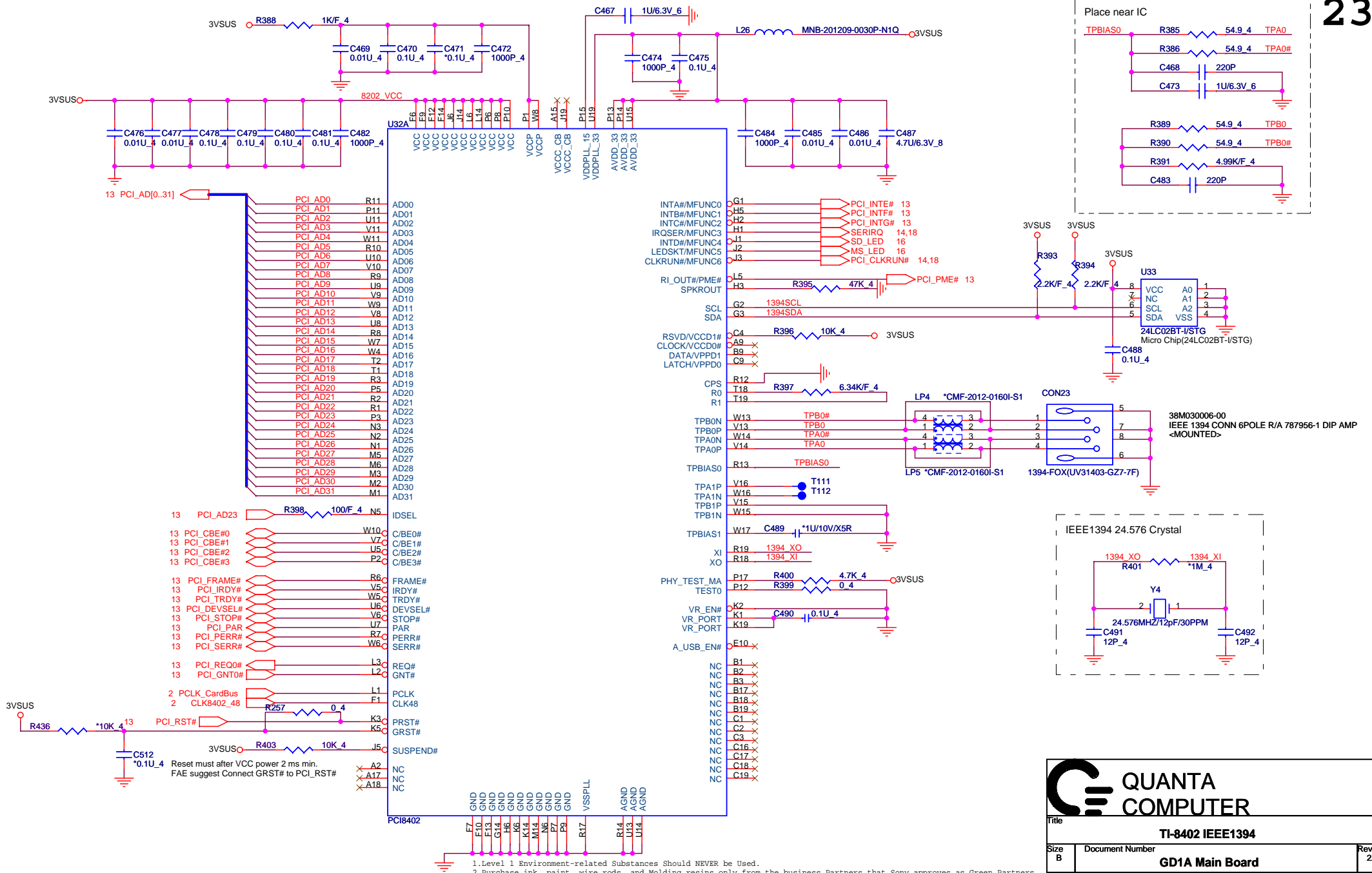
1

USBP7-

USBP+

X

FeliCa-PT1(AF706L-N2G11)



1. Level 1 Environment-related Substances Should NEVER be Used.  
 2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

**QUANTA COMPUTER**

Title: **TI-8402 IEEE1394**

Size B Document Number

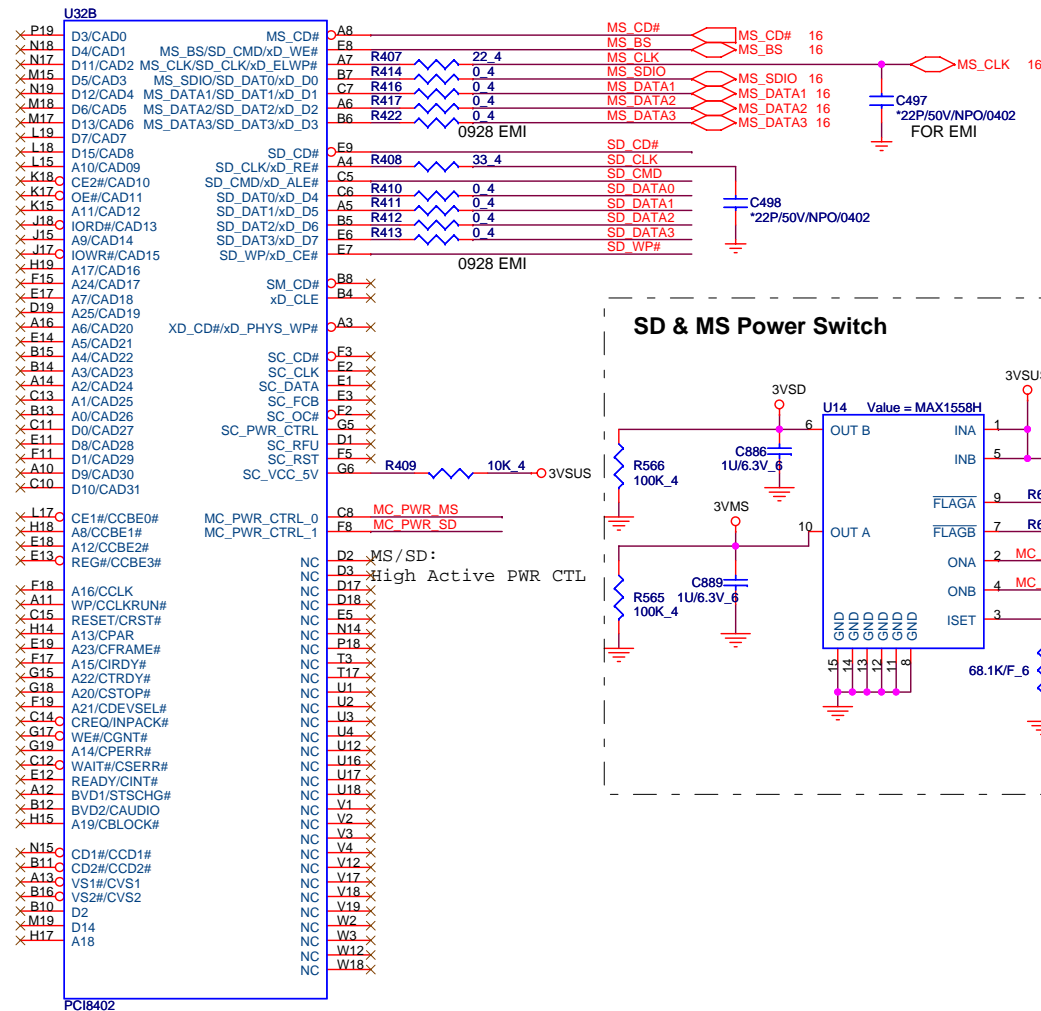
**GD1A Main Board**

Date: Monday, July 23, 2007

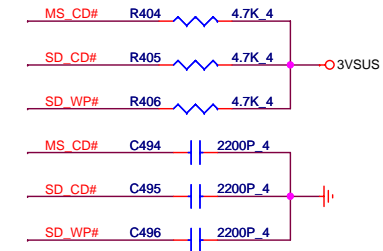
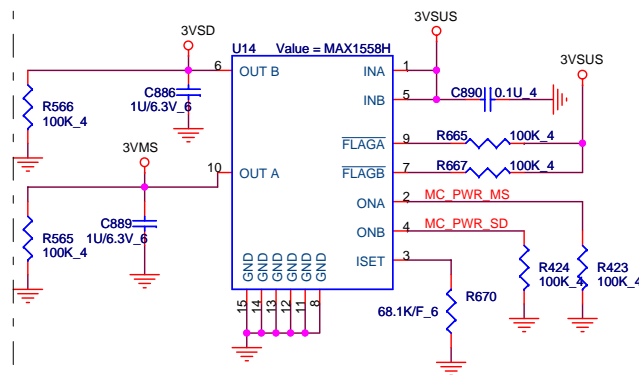
Sheet 23 of 35

Rev 2A

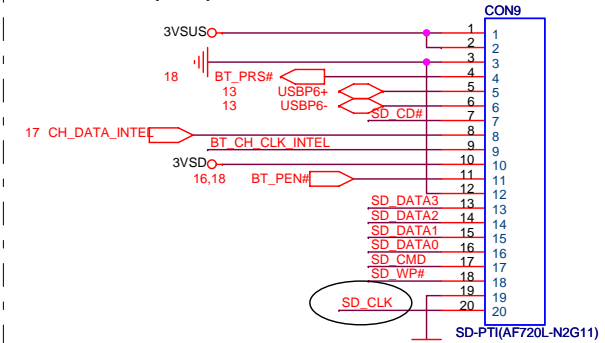




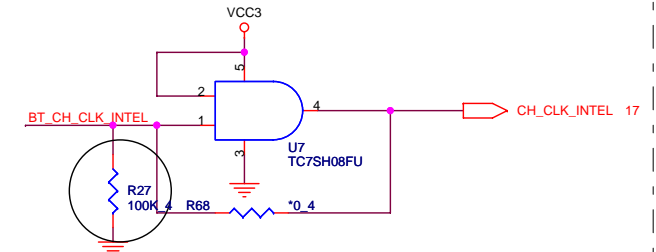
## SD &amp; MS Power Switch



## SD CON(FPC)



0711 Eric\_Delete R432, fixture of KB will damage it



0611 Eric\_install R27 for WL disconnecting issue

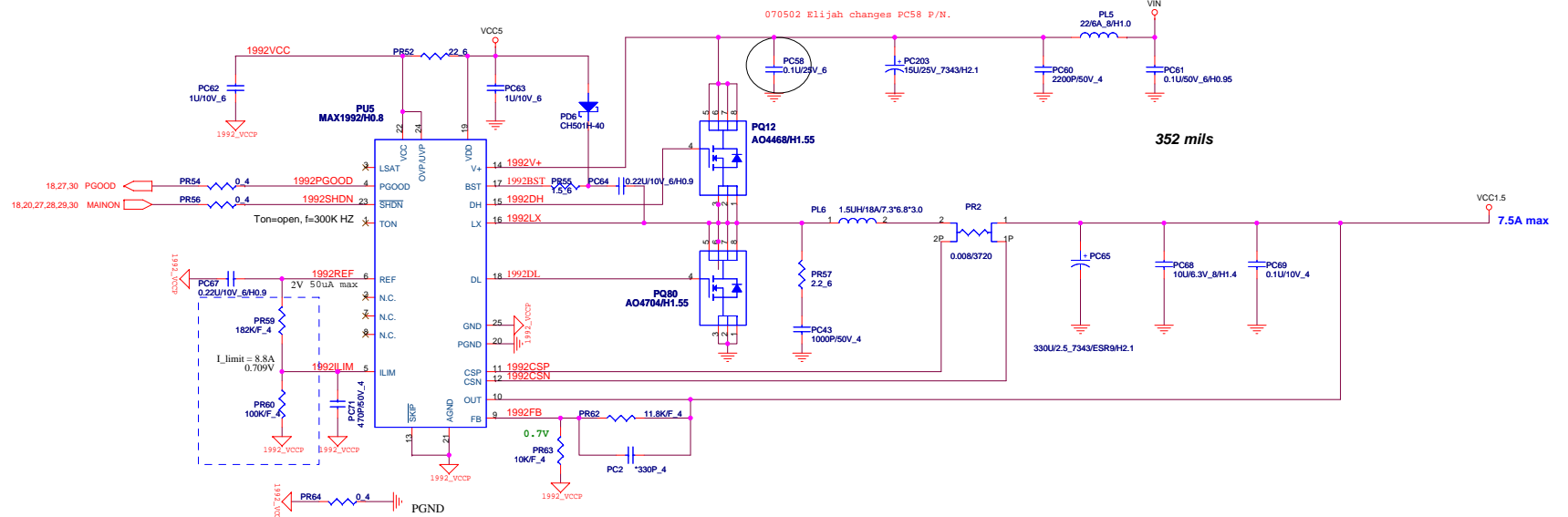


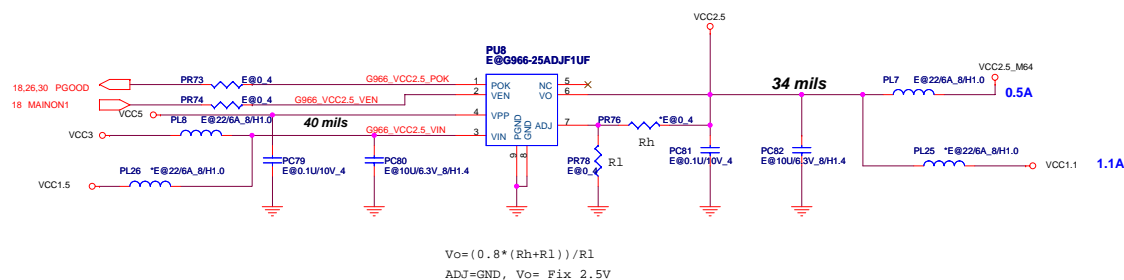
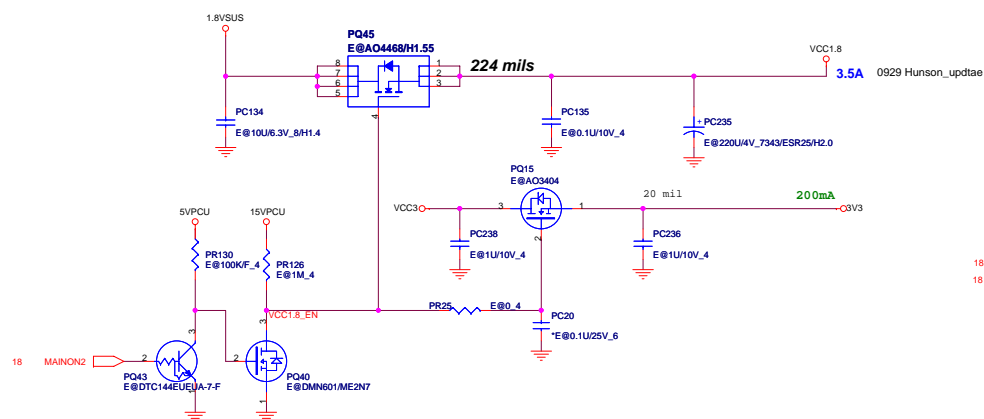
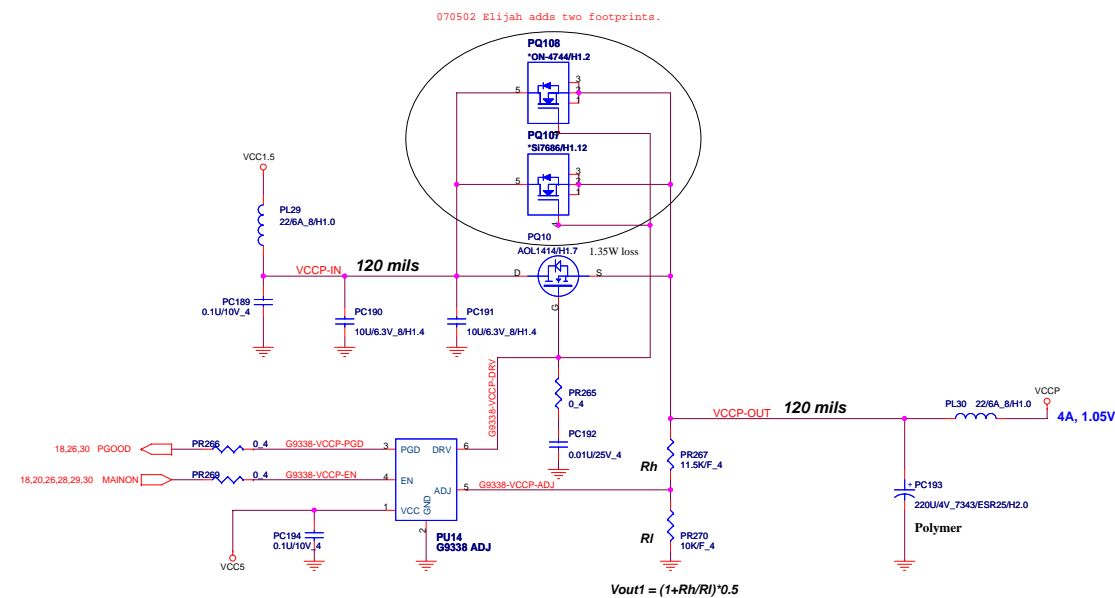
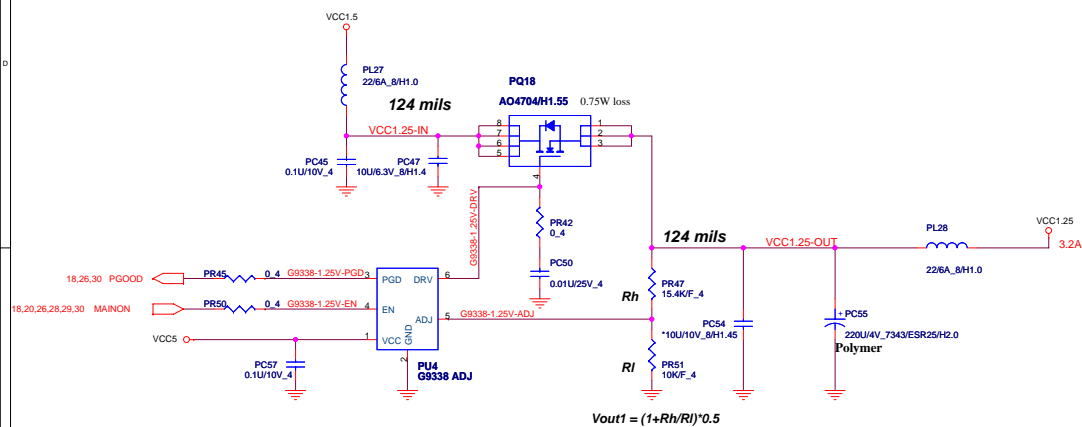
Title		TI-8402 MS & SD	
Size	Document Number	Rev	
B		3A	
		GD1A Main Board	
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- 1.Level 1 Environment-related Substances Should NEVER be Used.
- 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



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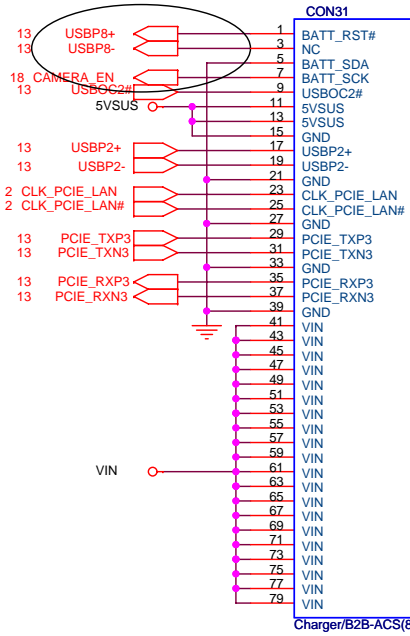




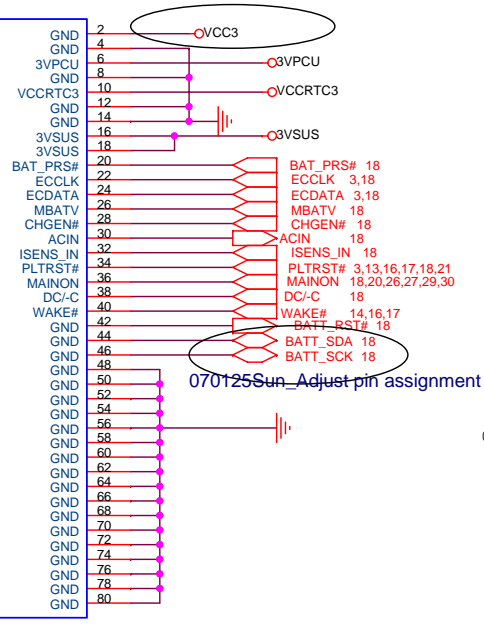
$$V_o = (0.8 \cdot (R_h + R_l)) / R_l$$

ADJ=GND,  $V_o$  = Fix 2.5V

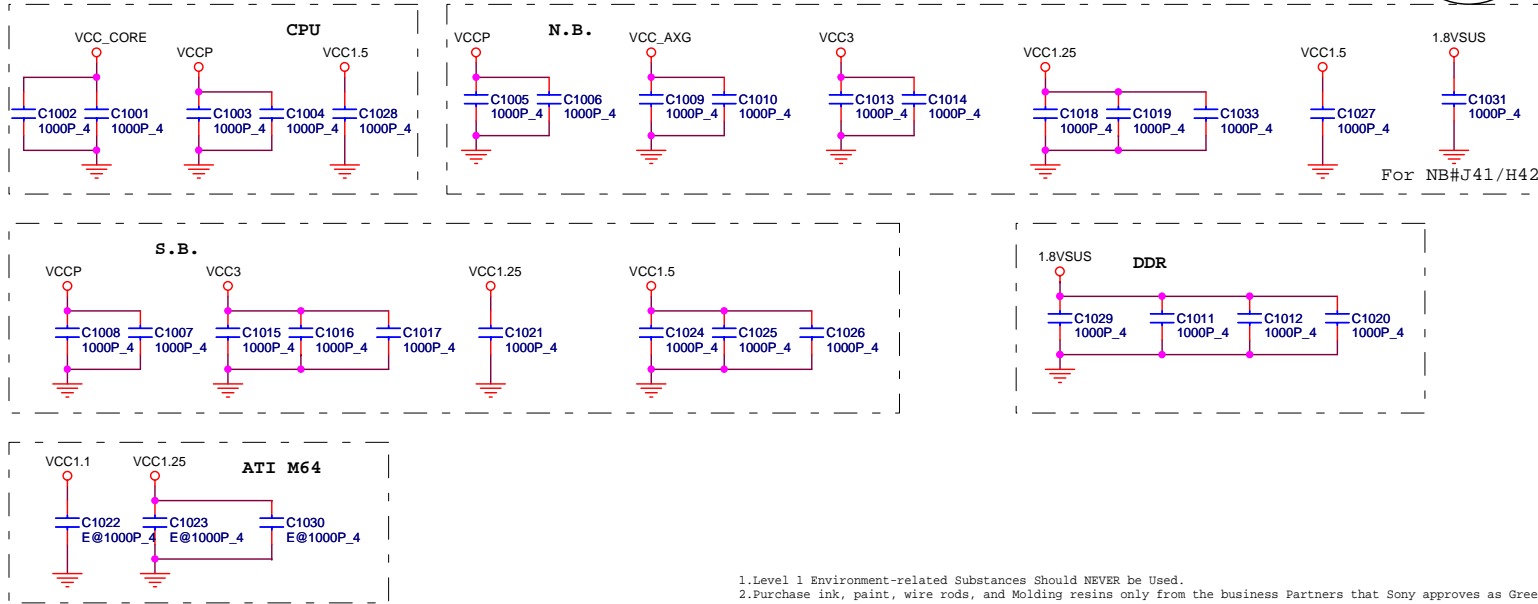
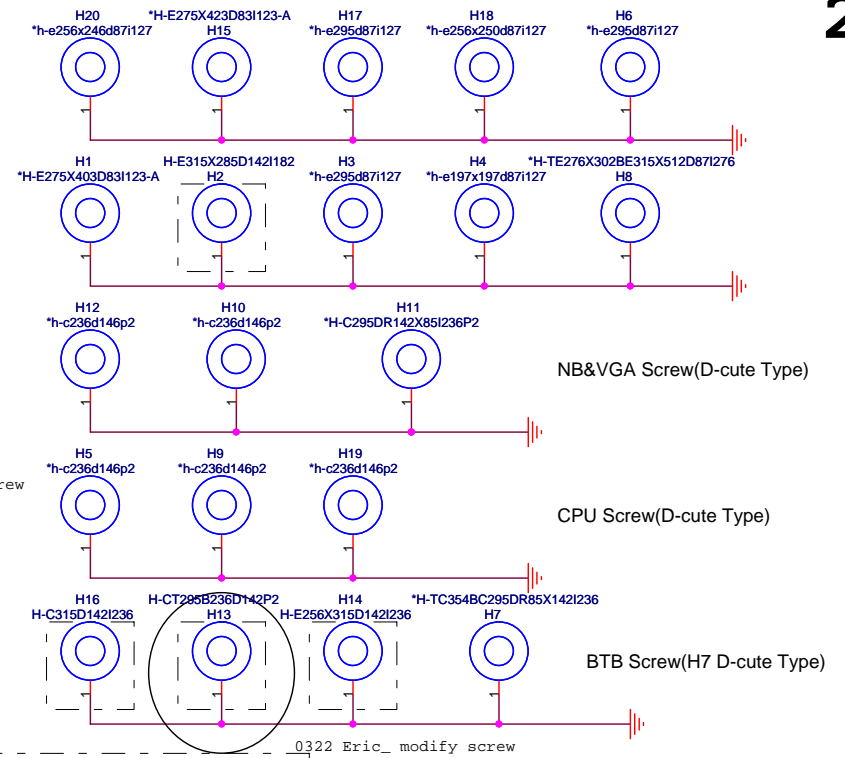
070125Sun\_Adjust pin assignment



070125Sun\_Adjust pin assignment



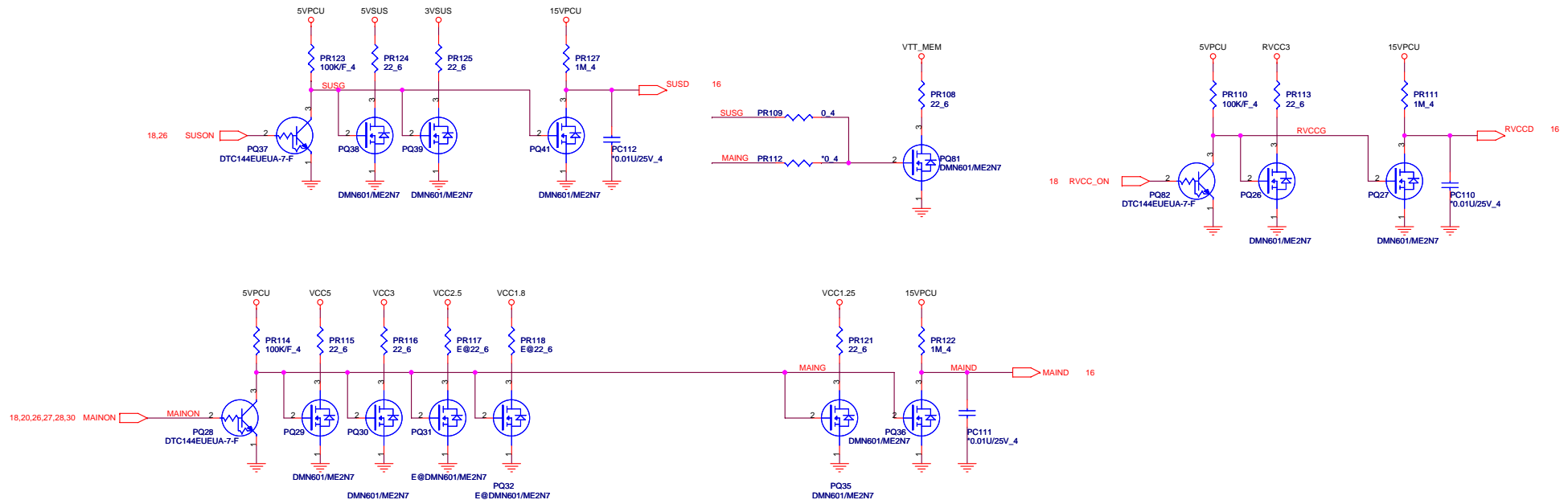
070125Sun\_Adjust pin assignment




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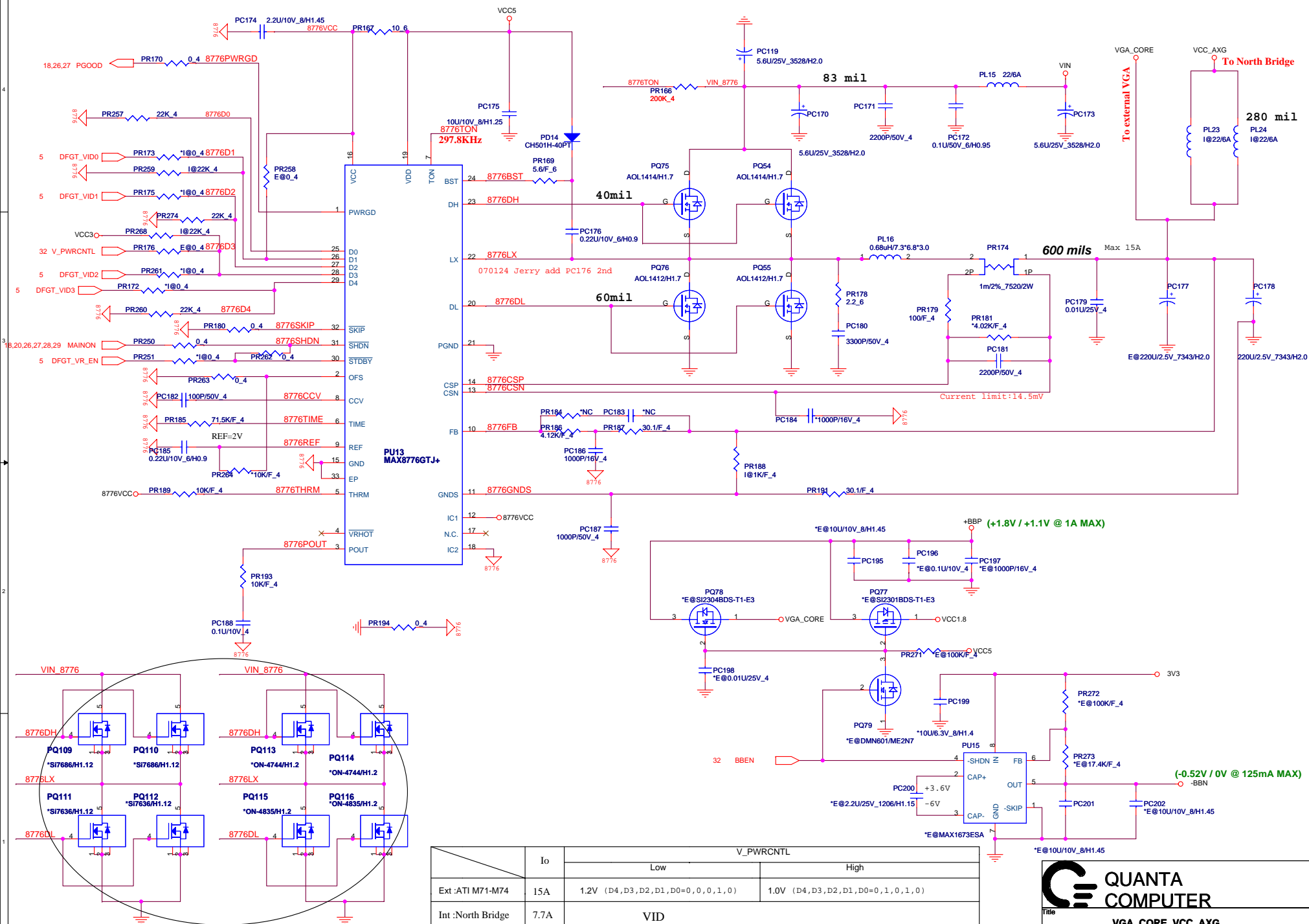
Title		
Power Charger & LAN CON		
Size B	Document Number	Rev 2A
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1. Level 1 Environment-related Substances Should NEVER be Used.
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		QUANTA COMPUTER	
Title		Discharge, SUSG, RVCCD, MAIND	
Size	Document Number	Rev	
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070502 Elijah adds PQ109 - PQ116 footprints.

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**QUANTA COMPUTER**

Title: **VGA\_CORE, VCC\_AXG**

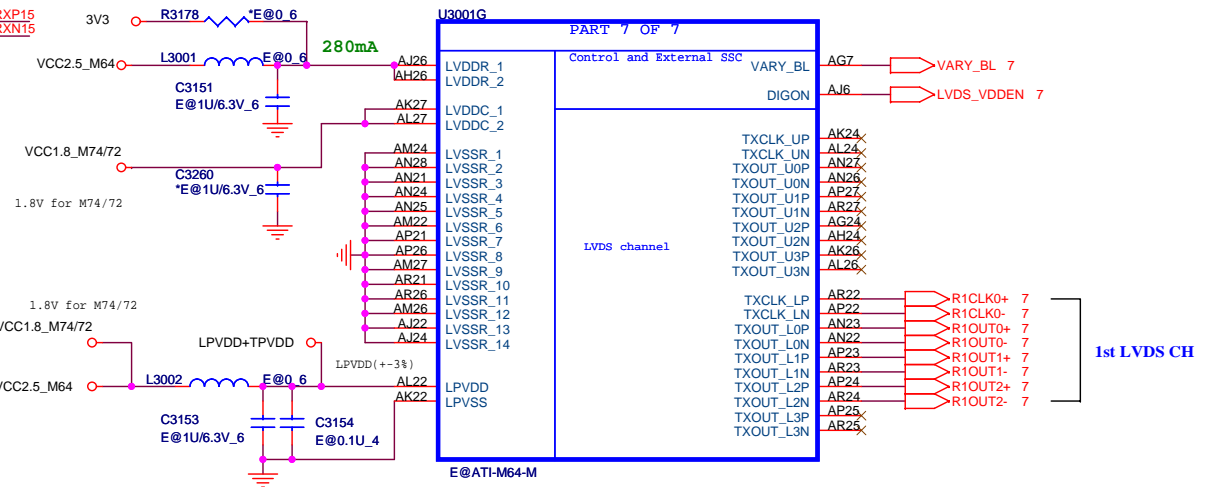
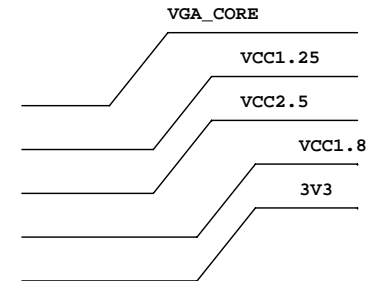
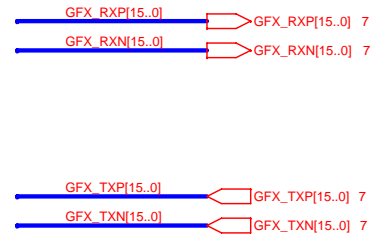
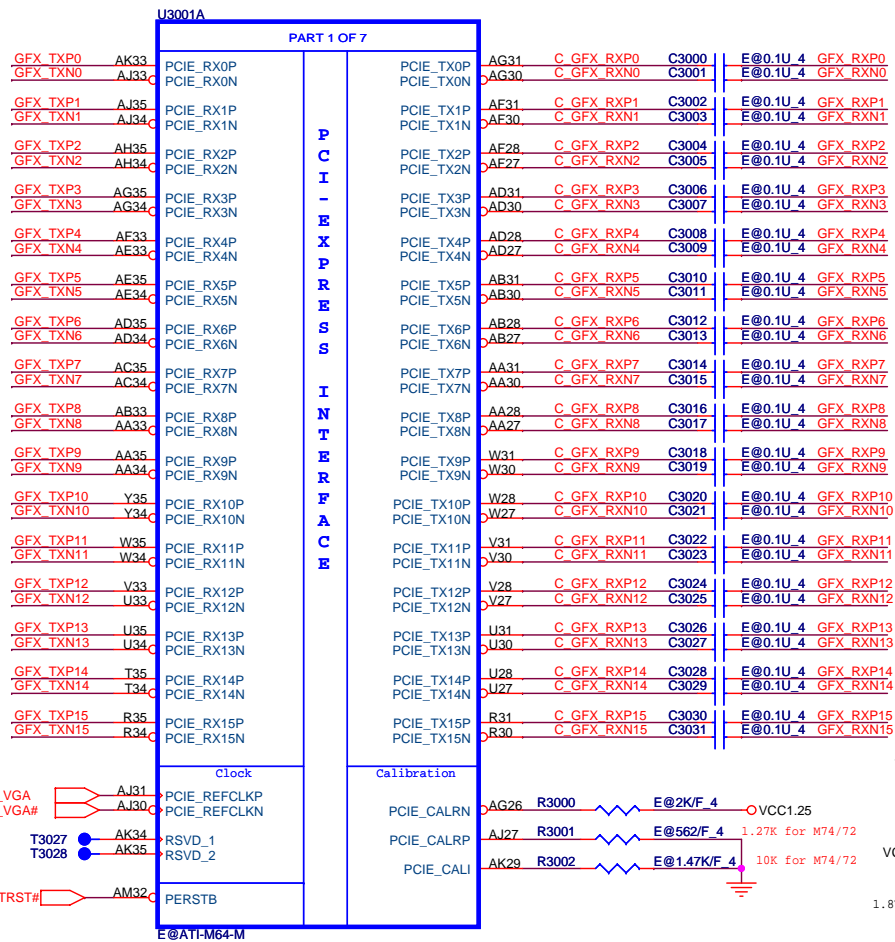
Size: Document Number

**GD1A Main Board**

Date: Monday, July 23, 2007

Rev: 2A

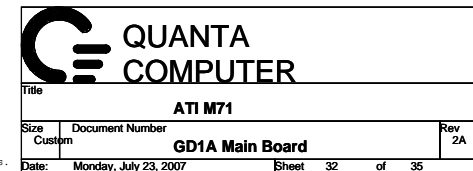
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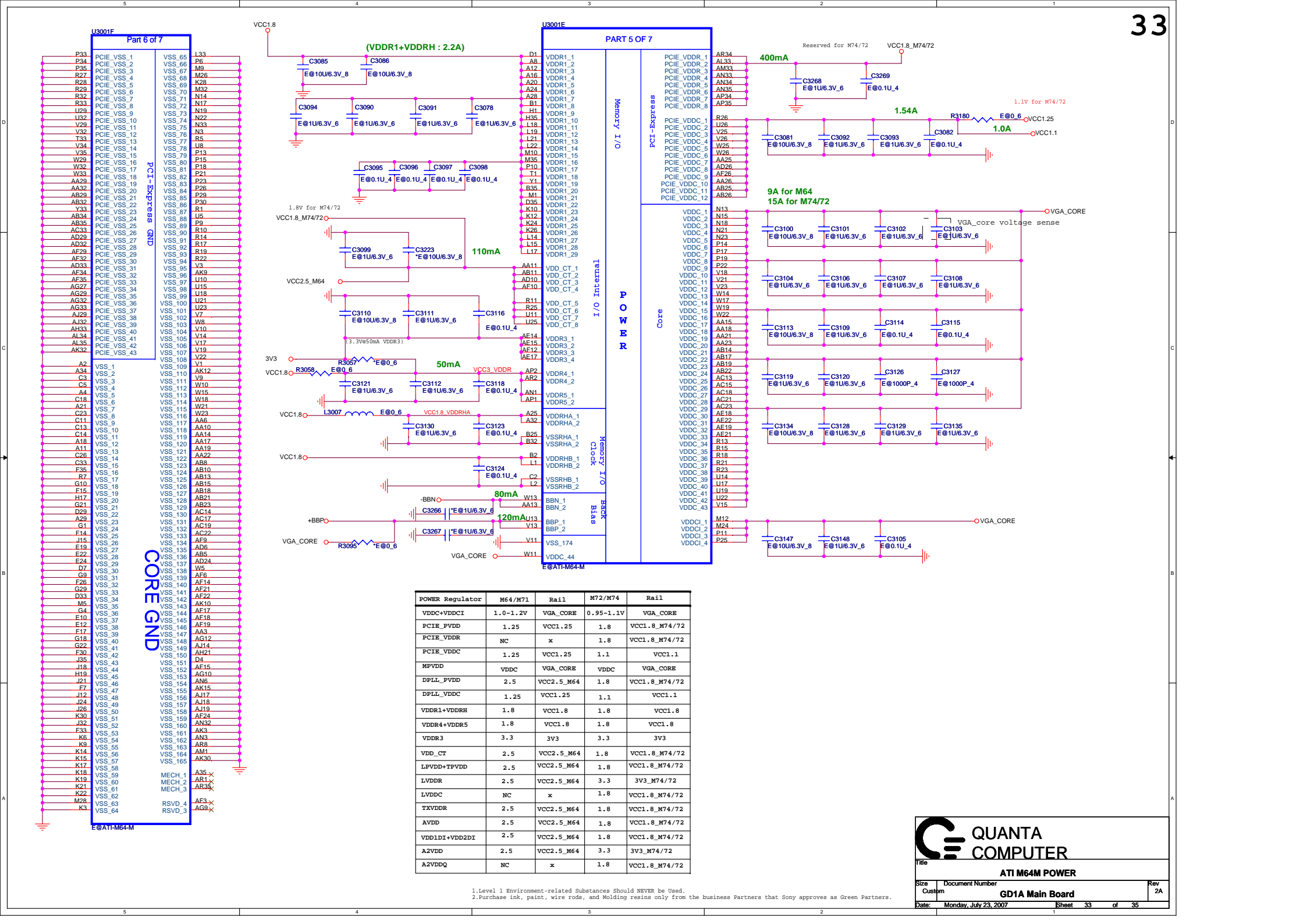


Title		
ATI M64M PCIE		
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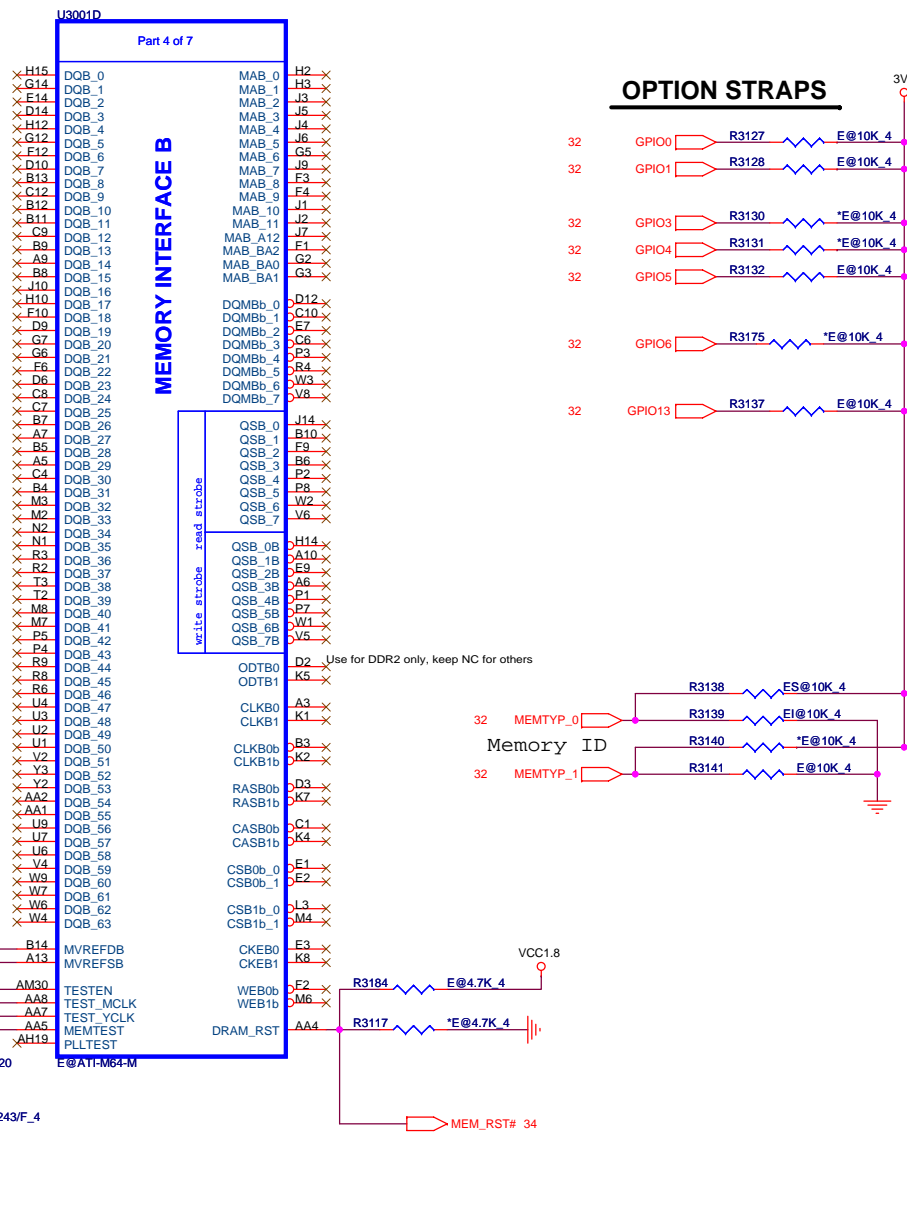


Title			
ATI M64M VRAM			
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Custom	GD1A Main Board	2A	
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## Channel B



## M64-M Strap

STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: full Tx output swing	0 (internal pull-down)
TX_DEEMPH_EN	GPIO1	(recommended) Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled (recommended)	0 (internal pull-down)
Reserved	GPIO(3:2)	ATI internal use only. Other logic must not affect this signal during RESET.(GPIO2=VDD_VCL)	00
DEBUG_ACCESS	GPIO4	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible	0 (internal pull-down)
PLL_IBIAS_RD	GPIO[6:5]	Bias Current for the PCI Express PHY PLL	01
Reserved	GPIO8	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM 0 Output from ROM)	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, controls chip IDIs. If rom attached identifies ROM type 000x - No ROM, MEM_AP_SIZE=00 128MB 001x - No ROM, MEM_AP_SIZE=01 256MB 010x - No ROM, MEM_AP_SIZE=10 64MB(Default) 011x - No ROM, MEM_AP_SIZE=11 Reserved 1000 - Parallel ROM, chip IDIs from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDIs from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDIs from ROM 1011 - Serial M25P10 ROM (ST), chip IDIs from ROM 1100 - Serial M25P05 ROM (ST), chip IDIs from ROM 1100 - Serial NX25F011B ROM (ISSI), chip IDIs from ROM	GPIO[9,13,12,11] 0000 (internal pull-down)
VIP_DEVICE	VSYNC	Indicates if any slave VIP host devices drove this pin low during reset. 0- Slave VIP host port device present. 1-No slave VIP port devices reporting presence during reset	0 (internal pull-down)
Reserved	PCIE_TEST	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM 0 Output from ROM)	0
Reserved	HSYNC	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM 0 Output from ROM)	0

## VRAM Straps

REV. 0.1

STRAPS	PIN	DESCRIPTION	VALUE
MEMTYPE[1:0]	GPIO 27,26	Memory identification for BIOS 00 - Infineon GDDR3 : 2M x 32 bits x 4 banks(Default) 01 - SAMSUNG GDDR3 : 2M x 32 bits x 4 banks 10 - RESERVED 11 - RESERVED	00

MEMTYPE1	MEMTYPE0	R3140	R3141	R3138	R3139	
0	0	NC	10K	NC	10K	00 - Infineon GDDR3 : 2M x 32 bits x 4 banks
0	1	NC	10K	10K	NC	01 - SAMSUNG GDDR3(G) : 2M x 32 bits x 4 banks
1	0	10K	NC	NC	10K	10 - Hynix GDDR3: 2M x 32 bits x 4 banks
1	1	10K	NC	10K	NC	11 - SAMSUNG GDDR3(I) : 2M x 32 bits x 4 banks



Title			ATI M64-M STRAP		
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